Steering electronics, module design and construction of an all silicon DEPFET module

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Abstract

High energy physics experiments require detectors with an excellent imaging performance. The innermost part is often a pixel vertex detector with 2D position readout. The DEPFET pixel detector is an option for the International Linear Collider and will be used in the Belle II experiment at the SuperKEKB accelerator in Japan. Two barrel layers will be installed in a very confined space and hence, a dense packaging of sensors, read-out and steering chips is mandatory. A hard radiation environment is influencing the electronics at the location close to the interaction point.

The steering chips are controlling the DEPFET imaging devices. They need to provide fast signals to read-out the large sensitive areas in a high speed. Two generations of steering chips are characterized and tested for their radiation hardness in this work. A converter chip was designed to operate the read-out chip stand-alone, until the data compression chip is ready.

The DEPFET detector modules will be build in the novel all-silicon approach, where the read-out and steering chips are mounted upside down directly onto the detector silicon. The silicon area is also used to interconnect the chips with the imaging devices and the cables. A thinned sensor area reduces the negative influences of the material on the particle tracks, but results in fragile devices.

A flip-chip interconnection technology connects the chips to the detector and builds the all-silicon module. The technology has to be compatible with the thin and fragile DEPFET devices. Different flip-chip methods are evaluated in this dissertation. Many processes are only feasible for mass production and can't adopt to the flexibility requirements in research and development. Two processes, the gold-stud and solder ball bumping, meet the requirements and were deployed in the scope of this work. Several test prototypes have been successfully built with these processes.

Interconnecting the flip-chip mounted chips with the DEPFET array and the off-module cable connection on the detector modules is a further task addressed in this work. The special DEPFET technology limits the design complexity of the chip interconnection. A high power consumption of the read-out chips and the dense packaging of chips on the module are increasing the complexity furthermore.

In summary, this work has provided an important contribution to the development of the novel high resolution DEPFET vertex detector concept and has advanced the construction of the Belle II pixel vertex detector.

Zusammenfassung

Experimente in der Hochenergiephysik benötigen Detektoren mit exzellenten bildgebenden Eigenschaften. Ein zentraler Teil ist oft ein Pixel Vertex Detektor zur 2D Positionsbestimmung. Der DEPFET Pixel Detektor ist eine Option für den International Linear Collider und wird beim Belle II Experiment am SuperKEKB Beschleuniger in Japan eingesetzt werden. Zwei zylindrische Lagen werden auf kleinstem Raum montiert und ein kompakter Aufbau des Sensors mit den Auslese- und Steuerchips ist dadurch nötig. Nahe am Wechselwirkungspunkt herrscht eine starke Strahlung, die die Elektronik negativ beeinflusst.

Die Steuerchips müssen schnelle Signale erzeugen, um den großen aktiven Bereich des DEPFET Detektors schnell auslesen zu können. Zwei Generationen der Steuerchips wurden in dieser Arbeit charakterisiert und auf ihre Strahlenhärte getestet. Ein Konverterchip wurde entwickelt, um den Auslesechip bis zur Fertigstellung des Datenkompressionschips betreiben zu können.

Die DEPFET Detektor Module werden ausschließlich aus Silizium-Komponenten aufgebaut. Die Auslese- und Steuerchips werden direkt auf das Detektor-Substrat montiert, welches auch zu deren Verdrahtung verwendet wird. Die sensitive Fläche wird gedünnt, um den negativen Einfluss des Materials auf die Teilchenspuren zu minimieren.

Die Flip-Chip Verbindungstechnologie wird verwendet, um die Chips und das Anschlusskabel mit dem Sensor-Substrat zu verbinden. Die Technologie darf die zerbrechlichen und dünnen Detektoren nicht zerstören oder negativ beeinflussen. Verschiedene Methoden wurden analysiert. Die meisten Prozesse sind auf die Verarbeitung von Wafern optimiert und für den Einsatz in der Forschung und Entwicklung ungeeignet. Zwei Verfahren, das gold-stud und das solder ball bumping, erfüllen die Flexibilitätsvoraussetzungen und wurden im Rahmen dieser Arbeit eingesetzt. Mehrere Test-Prototypen wurden mit diesen Verfahren erfolgreich hergestellt.

Die Verdrahtung der Flip-Chip montierten Chips mit den DEPFET Zellen und dem Kabel auf dem Detektor-Substrat ist ein weiterer Teil dieser Arbeit. Die DEPFET Technologie erlaubt nur eine begrenze Anzahl Metalllagen. Der hohe Strombedarf und die Dichte der Elektronik erschwert die Verdrahtung zusätzlich.

Diese Arbeit liefert einen wichtigen Beitrag zur Weiterentwicklung des neuen, hochauflösenden DEPFET Vertex Detektor Konzepts und hat den Bau des Belle II Pixel Vertex Detektors vorangebracht.

Contents

1 Introduction

The search for the origin of the universe and the interactions that build our world has driven scientists for many centuries. The philosophical thought of all matter being build of a few indivisible particles has been formulated by the ancient Greeks, who called these particles atoms (Greek: $\acute{\alpha}\tau o\mu o$). The first discovery of a particle in the beginning of the 19th century started the successful search in the field of particle physics. Many discovered particles could be explained as a combination of elementary particles. The theoretical Standard Model of particle physics has been formulated and predicted many elementary, subatomic particles. While most of them have been confirmed experimentally, the Higgs boson, as the key ingredient of the Standard Model, has not been discovered yet. It is required to give particles their mass. New particle accelerators reaching very high center of mass energies are needed to produce the rare events to confirm the existence of the Higgs. The Large Hadron Collider (LHC) is an energy frontier machine build at the European Organization for Nuclear Research (CERN[1]). New particle discoveries are expected in proton-proton collisions with a center of mass energy of 14TeV.

Energy frontier machines can discover new particles, but lower energy accelerators are needed to study the properties of particles in detail. The International Linear Collider (ILC) is currently developed to provide such a high precision at the Terascale. Particles discovered at the LHC can be analyzed in more detail in the electron-positron collider at energies of up to 1TeV.

The questions of how the universe evolved and why it is dominated by matter are addressed by flavor physics at B-factories like the Belle experiment at the KEKB accelerator in Japan. The charge-parity (CP) symmetry needs to be violated in order to explain the dominance of matter over antimatter in the universe. B-mesons created in the asymmetric electron positron colliders are precisely measured and can give an insight on CP violation. KEKB has rather moderate center of mass energies of 10GeV, but provides a 50 times higher interaction rate compared to the ILC, which allows the observation of phenomena with high statistics to either further support the assumptions of the Standard Model or to unveil new particles and processes beyond it. The rare/precision frontier will be enlarged by the SuperKEKB, an upgrade of the KEKB accelerator. An upgrade of the Belle detector is also necessary in order to cope with the high luminosity of the SuperKEKB.

Semiconductor sensors can provide the required precision to the ILC and Belle II detec-

[1] **C**onseil **E**uropéen pour la **R**echerche **N**ucléaire

tors. The main advantages of the semiconductor sensors, compared to other detector types like gaseous detectors, are a faster response time, a lower energy threshold and a smaller feature size. They allow the integration of many sensor devices on one piece of silicon and to obtain a high resolution image. Especially the DEPFET detector, with its integrated first amplification stage, achieves a spacial resolution of a few micrometers. The higher resolution demands a high density interconnection technique to connect the steering chips to the sensor and to transfer the sensor information to the readout chips. The detectors need to be placed as close as possible to the accelerator's interaction point to reconstruct the particle tracks as precise as possible.

A harsh radiation environment is influencing the detectors at the position close to the interaction point. They need to be read out more often in order to reduce the amount of false hits in a data set and to allow a precise track reconstruction. The steering chips need to provide fast control signals to the matrix and both, the readout and steering chips, have to be radiation hard. The results of the chip characterization and irradiation tests are presented in chapters 4 and 5.

A dense packaging of sensor, steering and read-out devices, together with cabling, cooling and mounting infrastructure is mandatory for an inner layer pixel detector. Particles passing through matter are interacting with nuclei and changing their trajectories. The amount of material has to be reduced in order to limit the number of interactions, resulting in small, thin and fragile devices. Read-out and steering chips have to be mounted on those fragile devices. The density requirements of such a novel all-silicon detector module can be accommodated by flip-chip mounting of the chips directly onto the detector silicon. This interconnection technology utilizes different conductive materials, such as gold or solder, to form the conductive paths between chips and substrate. Gold and solder ball placement processes have been evaluated and set-up during this thesis and the results are presented in chapter 6.

The detectors are arranged in concentric layers around the particle interaction point, limiting the size of the detector silicon. As most of its area is devoted to the imaging pixels, only a small fraction is available for mounting and interconnecting the read-out and steering chips to the off-module cable connection. Additionally, the DEPFET detectors are manufactured in an engineering process with a confined design complexity. Providing the high power and signal routing demands in such an environment is challenging. The results of the design efforts for the all-silicon module are presented in chapter 7.

2 DEPFET Active Pixel Sensor Basics

The DEPFET[1] is a monolithic active pixel semiconductor sensor with a very good signal-to-noise ratio. This makes the DEPFET an attractive device for spectroscopy applications or particle physics, where a high spacial resolution and low power consumption are needed. The principle of the DEPFET was shown by Kemmer and Lutz in 1987 [1].

Detectors built with semiconductor material have the advantage of a large signal-to-noise ratio, which allows the detection of low energy radiation. They also allow the integration of electronics within the detector. The short, low capacitance path from signal source to electronics enables the device to amplify the signals with low noise contribution. Hit detection or timestamp counter circuits are integrated in monolithic active pixel detectors.

DEPFET detectors are developed for X-ray imaging in the IXO[2][2] astronomy project or for the European XFEL[3][3] for atomic and molecular spectroscopy. They are also an option for the ILC[4] and for Belle II particle physics experiments as the inner layer vertex detectors. ILC is a e^+e^- linear accelerator, with energies up to $500GeV$. Belle II is an asymmetric electron-positron collider to study B-physics.

2.1 Radiation Detection

Radiation is detected because of its interaction with matter. It looses its energy partly or completely through interaction processes while traversing through matter. The interactions create free electrons, either by direct or indirect processes, which can be detected as electrical signals. Depending on the type of radiation, different processes are involved. It is distinguishable between charged particles and photons.

2.1.1 Charged Particles

Charged particles interact with matter by different processes, like inelastic collisions with atomic electrons, elastic scattering from nuclei, emission of Cherenkov radiation and

[1] **Dep**leted **F**ield **E**ffect **T**ransistor
[2] **I**nternational **X**-ray **O**bservatory
[3] **X**-ray **F**ree **E**lectron **L**aser
[4] **I**nternational **L**inear **C**ollider

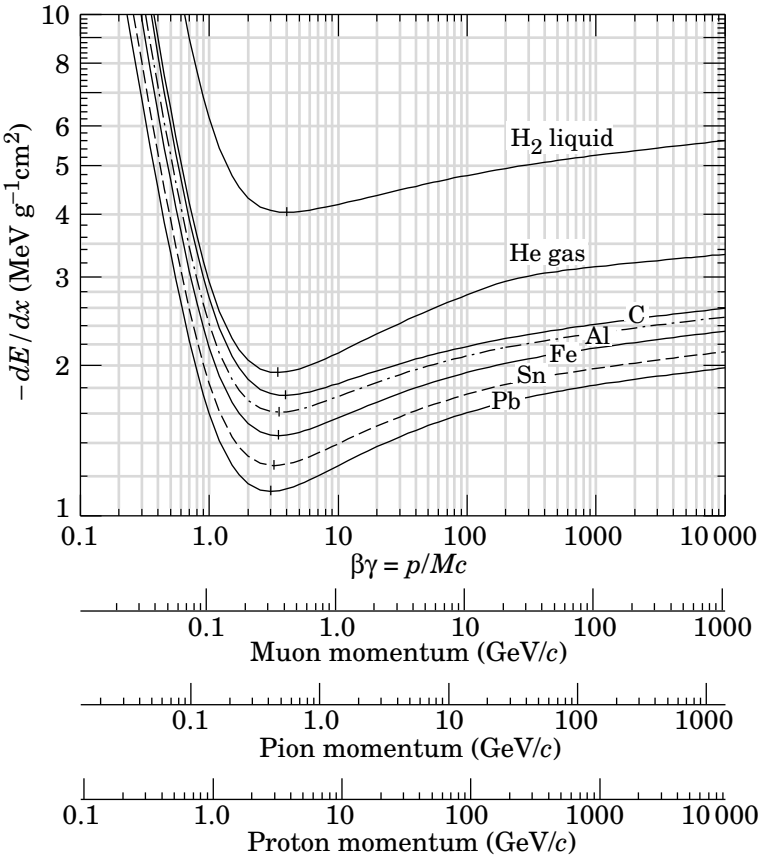

Figure 2.1: Mean energy loss in different materials as a function of particle momentum by the Bethe-Bloch formula. [4]

bremsstrahlung. The type of interaction of charged particles depends on their mass. Energy loss of charged particles heavier than electrons is mainly caused by inelastic collisions with atomic electrons causing ionization or excitation. In a single collision, only a small amount of kinetic energy is transferred. Due to the density of matter, the amount of collisions are high enough to loose a significant amount of energy. Electrons and positrons transfer most of their energy by bremsstrahlung. They emit a photon when they are decelerated by the electric field of an atomic nuclei.

The mean energy loss in matter of heavy, charged particles with an intermediate energy caused by ionization or excitation processes is described by the Bethe-Bloch formula[4][5]:

$$-\left\langle \frac{dE}{dx} \right\rangle = Kz^2 \frac{Z}{A} \frac{1}{\beta^2} \left[\frac{1}{2} ln \frac{2m_e c^2 \beta^2 \gamma^2 T_{max}}{I^2} - \beta^2 - \frac{\delta(\beta\gamma)}{2} \right]$$

where

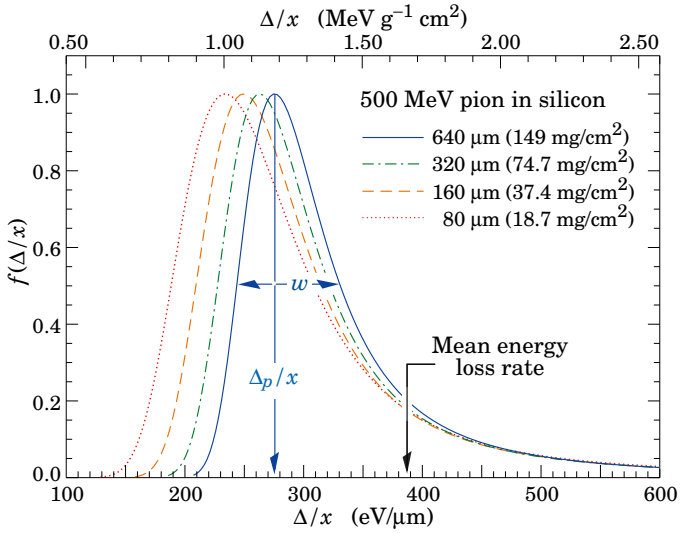

Figure 2.2: Landau distribution for different silicon thicknesses. [4]

$\frac{dE}{d}$ energy loss of the particle, usually given in $\frac{eV}{g/cm^2}$

K $4\pi N_{Av} r_e^2 m_e c^2 = 0.307075 MeV\,cm^2$

z charge of the traversing particle in units of the electron charge

Z atomic number of the absorption medium (14 for silicon)

A atomic mass of the absorption medium (28 for silicon)

$m_e c^2$ rest energy of the electron ($0.511 MeV$)

β velocity of the traversing particle in units of speed of light

γ Lorentz factor $1/\sqrt{1-\beta^2}$

I mean excitation energy ($137eV$ for silicon)

T_{max} maximum kinetic energy transferred to a free electron by collision

$\delta(\beta\gamma)$ density effect correction to ionizing energy loss for high particle energies

Figure 2.1 shows the mean energy loss for different absorber materials as a function of particle energy, calculated by the Bethe-Bloch formula. For low energies, the $1/\beta^2$ term is dominant and the stopping power decreases to a minimum. This minimum is reached with particle velocities about 0.96 the speed of light. With further increasing energy, dE/dx rises again due to the logarithmic term. A particle with an energy in the minimum of the Bethe-Bloch formula is called minimum ionizing particle (MIP).

For thick absorbers, the energy loss probability distribution is of Gaussian shape centered around the mean value given by the Bethe-Bloch formula. However thin layers of matter, which are commonly used in particle physics, have a energy loss probability distribution

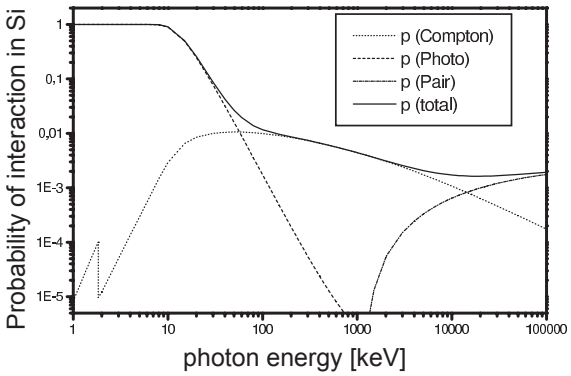

Figure 2.3: Probability of energy loss of a photon in silicon. [6]

with a long tail to higher energies. Fluctuations of energy loss for thin absorbers are described by the Landau distribution. Fast particles pass through the sensor, don't deposit all their energy, but generate δ-electrons. δ-electrons (also named knock-on electrons) are high energy free electrons which are ionizing themselves and thus create more charge by secondary ionization.

Figure 2.2 shows the Landau distribution for different silicon thicknesses. The most probable stopping energy in a $75\mu m$ detector is $\approx 18keV$, corresponding to $\approx 4800e^-$.

2.1.2 Photons

Photons are neutral and interact with matter differently than charged particles. The main interaction processes are:

- **Photoelectric effect:** The photon is absorbed by an atomic electron which gains the photon's energy. If its energy is higher than the electron's binding energy, the electron is ejected from the atomic shells. The free electron's kinetic energy is $E = hf - \varphi$, where h is the Planck constant, f the frequency of the photon and φ the work function. The kinetic energy of this electron will be transferred by ionizing collisions to the absorber material.
- **Compton scattering:** A photon is scattered elastically on an electron and causes an energy transfer to the electron. The electron is then ejected from the atomic shell. The amount of energy transfer depends on the photon's energy and the scattering angle. The transfer is maximum for backscattering, when the photon is reflected.
- **Pair production:** The high-energy photon is converted into a electron-positron-pair by interacting with a nucleus. A photon energy of at least twice the rest energy of an electron is needed: $2m_ec^2 = 1.022MeV$.

At energies below $60keV$, the photoelectric effect dominates in silicon material. Higher energy photons predominantly interact through Compton scattering. Above $10MeV$, pair production is dominant [7]. Figure 2.3 shows the probability of energy loss in silicon as a function of the photon's energy for the above mentioned interaction processes.

Photons are either absorbed or scattered by a large angle and thus removed from the photon beam. A photon that has passed through the material and didn't interact with it, hasn't lost energy. The beam doesn't loose energy, but intensity. The intensity loss of a photon beam passing through matter shows exponential behavior as a function of material thickness:

$$I(z) = I_0 e^{-\mu z}$$

where μ is the absorption coefficient and depends on the density of the material and the beam energy. z is the thickness of the absorber.

2.2 Semiconductor Sensors

Semiconductor sensors have many advantages for detecting radiation or ionizing particles. The small band gap allows an electron to be lifted from the valence to the conduction band and thus creates an electron-hole pair with only a few eV. This is much lower than in gaseous detectors: A mean value of $3.63eV$ in silicon, compared to approximately $30eV$ in gas, is needed for ionization. Hence, a much better energy resolution and lower signal-to-noise ratio is achieved.

Semiconductor material has a high density, which results in a higher stopping power. The sensor thickness can be lower than in other detector types without decreasing the sensor performance. A fast charge collection time enables the device to be read out with faster frame times. The bulk of the detector can be fully depleted by using a high resistivity and weakly doped substrate. The generated charge cannot recombine and thus can be completely measured.

2.2.1 The PN-Junction as a Detector

The basic element of a silicon sensor is a pn-junction with a fully depleted bulk. In a fully depleted bulk, no free charge carriers are available and an electron-hole-pair, that has been generated by ionization, cannot recombine. It will be separated by the electric field and moves towards the electrodes, where a signal is measured.

The device is created by using a weakly n-doped silicon material and implanting a highly doped p-type area on one side (see figure 2.4). The difference in majority charge carrier concentrations causes a diffusion of electrons into the p-doped region and holes into the

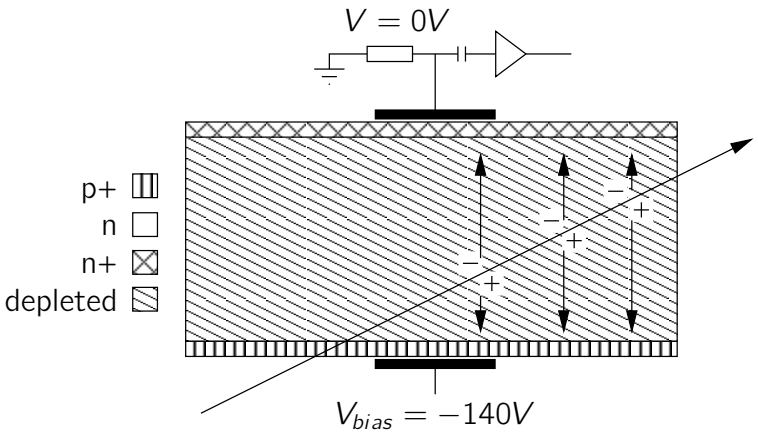

Figure 2.4: PN-junction as detector. [7]

bulk. A depletion zone starts to grow in which the bulk is positively charged, due to the missing electrons. The p-implantation is negatively charged, due to missing holes. This charge creates an electric field counteracting to the diffusion until it reaches an equilibrium. The corresponding potential is called *built-in voltage* V_{bi}.

The size of the depletion zone in equilibrium can be enlarged by applying a voltage with the same direction as the electric field. It is called reverse bias voltage, as it has the opposite polarity to the conducting direction of a pn-diode. The reverse voltage increases the electric field and removes more majority charge carriers. Due to the difference in doping concentrations, the depletion zone reaches much more into the weakly doped n-type bulk than into the p-doped region. By increasing the voltage, the depletion zone grows until the bulk is fully depleted.

The total width W of the depletion zone can be calculated as followed [5]:

$$W = \sqrt{\frac{2\varepsilon_0\varepsilon_{Si}}{e}\left(\frac{1}{N_A}+\frac{1}{N_D}\right)(V_{bias}+V_{bi})}$$

A typical donor concentration of the DEPFET detector is $N_D \approx 10^{12} cm^{-3}$ for the bulk material and $N_A > 10^{19} cm^{-3}$ for the acceptor concentration of the p-implantation. As $N_D << N_A$ and $V_{bias} >> V_{bi} \approx 0.6V$, the terms $1/N_A$ and V_{bi} can be neglected. The required bias voltage to fully deplete a bulk of width W is:

$$V_{bias} \approx \frac{eN_D}{2\varepsilon_0\varepsilon_{Si}}W^2$$

For the above given donor concentration, a $450\mu m$ thick silicon needs a depletion voltage of $\approx 130V$. However, voltage can be reduced to $\approx 3.75V$ by using a $75\mu m$ thin device.

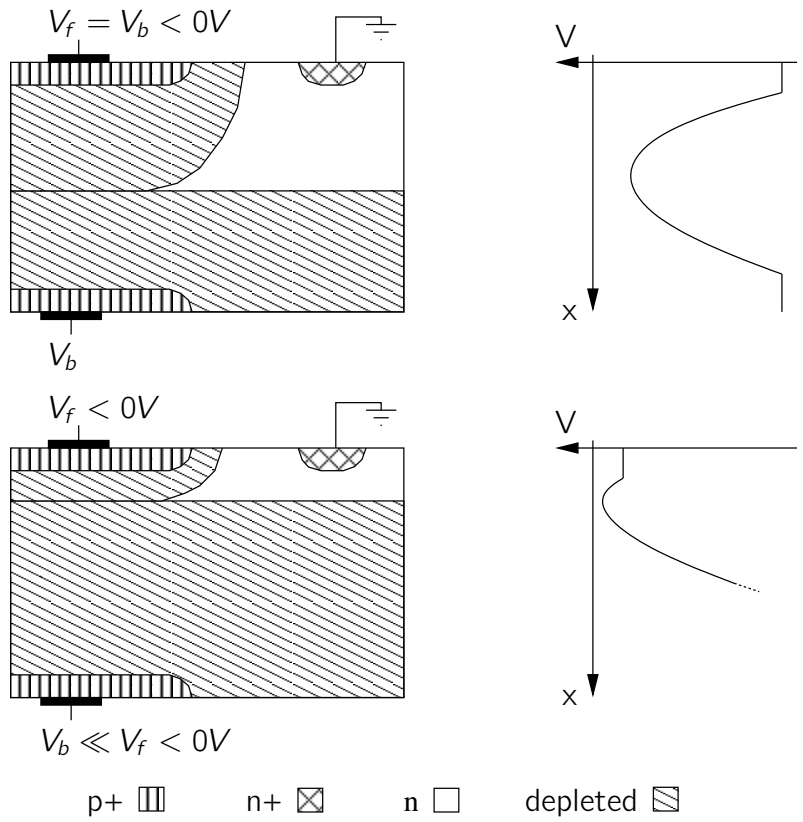

Figure 2.5: Principle of sidewards depletion. [7]

2.2.2 Principle of Sidewards Depletion

The principal of sidewards depletion has the advantage of creating a potential minimum for electrons within the bulk material by influencing the electric field.

This is achieved by creating highly p-doped implantations on both sides of the weakly n-doped material and adding a bulk contact at one side (see figure 2.5). The bulk contact is kept at ground potential, whereas both p-contacts are connected to a negative voltage. Depletion zones are reaching into the bulk from both pn-junctions. By applying the same voltage to both p-contacts, the potential minimum is in the middle of the material. In order to completely deplete the bulk from two sides, only a fourth of the bias voltage of a single pn-junction is required. Lowering the voltage on one side and increasing it on the other shifts the minimum towards surface with the lower voltage.

The Poisson-equation describes the potential perpendicular to the substrate surface[7]:

$$\frac{\delta^2 \Phi(z)}{\delta z^2} = -\frac{\rho}{\varepsilon_0 \varepsilon_r}$$

It is solved by:

$$\Phi(z) = \frac{\rho}{2\varepsilon_0\varepsilon_r} z(d-z) + \frac{z}{d}(V_b - V_f) + V_f$$

with the back side potential V_b, the front-side potential V_f and the substrate thickness d. The potential minimum is located at:

$$z_{min} = \frac{d}{2} + \frac{\varepsilon_0\varepsilon_r}{\rho d}(V_b - V_f)$$

The position of the minimum within the bulk is defined by the front side and back side potentials.

2.2.3 Radiation-Induced Effects

In MOS transistors and semiconductor sensors, radiation deteriorates the performance of the device. Sensors are affected by type inversion, an increase of leakage current and charge trapping. MOS transistors show a shift in threshold voltage, a reduced mobility of charge carriers and also an increased leakage current.

The bulk of semiconductor sensors is damaged by particles, which do not interact only with electrons and thereby create signals, but also interact with the silicon's nuclei. Silicon is a crystal and interacting particles will remove atoms from their lattice position. This creates crystal defects, that can be electrically active and change the detector's behavior.

In order to remove an atom from its lattice position, a recoil energy of $25eV$ is required. To provide this energy, an electron needs at least $260keV$, protons and neutrons need only $190eV$, because of their higher mass [5]. If the removed lattice atom gets enough energy transferred by the collision, it will also cause defects by secondary interactions. When the transferred energy exceeds about $2keV$, the atom creates defects in a small area. These cluster defects are mostly created by neutrons, because they interact with the nuclei and are not scattered electromagnetically. Charged particles are screened by the lattice atom's electrons and thus create mostly point defects.

Non-ionizing energy loss (NIEL) is used as a measure in order to compare the damages caused by different particles at different energies. It describes the energy deposited in the material, that is not used for signal generation by ionization. Neutrons with $1MeV$ are used as a reference. A hardness factor converts the physical fluence of a particle to the equivalent of $1MeV$ neutron fluence.

Defects are able to move within the silicon material and create secondary point defects by combining with other defects. They can be stable and change the electrical properties of the material. It is also possible, that the defects anneal during their movement. Point defects and trapped holes near the Si/SiO_2 interface create energy levels in the band

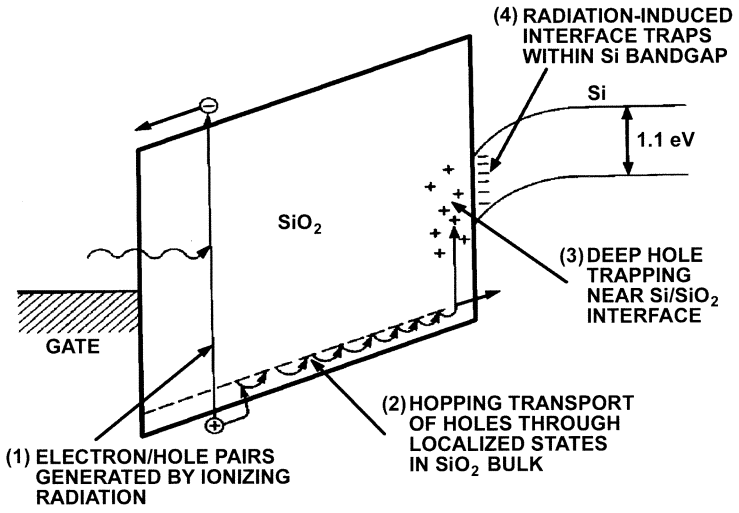

Figure 2.6: Energy band diagram showing the main processes of radiation-induced charge generation. [8]

gap, that allows electrons to switch more easily to the conduction band and thus create an increased leakage current.

Electrically active point defects influence the effective doping, which is the difference between n- and p-like doping effects. The defects act like p-doping and reduce the initial effective n-doping of the bulk. This allows the full depletion of the material with a lower reverse bias voltage. It decreases up to a flux of $\Phi = (2-5)10^{12} cm^{-2}$ where the n- and p-doping effects cancel each other and the material behaves like intrinsic silicon. With a more increasing flux, the n-material starts to behave like p-doped material. This is called *type inversion*. The pn-junction is now at the n^+-side of the detector and depletion zone starts to grow from there.

Similar to all MOS transistors, the DEPFET is also susceptible to threshold voltage shifts caused by charge build up in the gate oxide. Ionizing radiation creates electron-hole pairs in the oxides. If a positive voltage is applied at the gate electrode, the charge is separated, the electrons drift towards the gate and the holes towards the Si/SiO_2 interface. Due to the higher mobility of electrons ($\mu_{n,oxide} \approx 20 cm^2/(Vs)$), they are removed from the oxide within picoseconds. Holes are less mobile ($\mu_{p,oxide} \approx 2 \times 10^{-5} cm^2/(Vs)$) and mostly remain near their generation point. They form a positive oxide-trap charge [8]. Other holes move through the oxide by hopping through shallow traps. Near the Si/SiO_2 interface, some holes fall into long-lived trap states and contribute to the voltage shift. Others are exited into the silicon substrate. While hopping through the oxide lattice structure, they release hydrogen ions (protons), that also move to the Si/SiO_2 interface and form interface-traps [9]. The effect is dependent on the bias voltage. If no bias is applied, the recombination of generated electron-hole pairs is most probable and thus less charge builds up in the oxide.

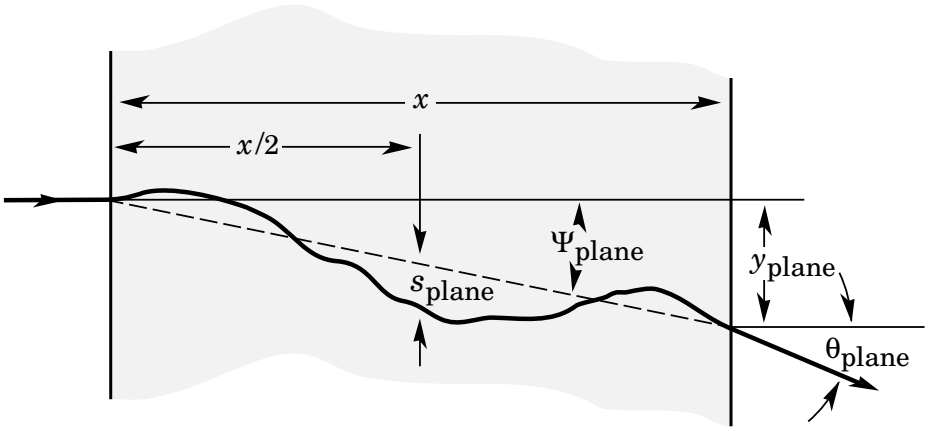

Figure 2.7: Multiple scattering of particle passing through matter. [4]

This additional charge necessitates compensation by an increased gate voltage, which results in the threshold voltage shift. Thinner gate oxides are less susceptible to threshold shifts, because the volume, where charge can be generated, is smaller. The thin gate oxides of deep sub-micron MOS technologies have very low threshold shifts: $\Delta V_T = Q_{OX}/C_{OX}$ leads to a voltage shift, that is proportional to t_{OX}^2. These technologies are 'intrinsically' radiation hard, because tunneling removes trapped oxide charges.

Not only the gate oxide of a transistor is sensitive to radiation damage, but also the much thicker field oxide around the transistor. The charge trapped in this oxide causes a parasitic leakage path from the source- to the drain-region by creating a conductive path. Current flows outside the active, gate controlled transistor area, even if the transistor is switched off. They increase the static power consumption of an integrated circuit.

Interface states between Si and SiO_2 result in an increased sub-threshold slope and a higher 1/f noise of the transistor.

Large concentration of trapped charge at the interface reduces the mobility of charge carriers in the transistor channel, which reduces the transconductance g_m. As a consequence, this decreases the drive capability of the transistor, degrades timing parameters and leads to a failure of the integrated circuit.

Oxide trapped holes are relatively stable, but may be removed through an annealing process, which can take hours or even years. Annealing is caused by tunneling and thermal excitation processes and is dependent on temperature, time and the applied electrical field. In tunneling, the hole is not removed, but neutralized by an electron tunneled from the silicon into the SiO_2.

2.2.4 Multiple Scattering

Multiple scattering is deteriorating the particle track reconstruction precision, as it influences the particle trajectory. Many elastic scatterings in the electric field of nuclei with small angled deflections cause large deviations from the original trajectory. Particles exit the material at different positions and with different angles (figure 2.7). Scattering is a stochastical process, where the width of the projected deflection angle can be approximated by a Gaussian distribution. It is dependent on the thickness x of the material, given in radiation length x/X_0, the momentum p, velocity βc and the charge number of the particle z:

$$\Theta_{plane} = \frac{13.6}{\beta cp} z \sqrt{x/X_0} \left[1 + 0.038 \, ln(x/X_0)\right]$$

Radiation length is the length of matter traversed by an electron or photon, which interacts with the material. It is the mean distance where an electron looses all but $1/e$ of its energy by bremsstrahlung and $7/9$ of a photon's mean free path[5] between pair productions. It is often given in $g\,cm^{-2}$. The radiation length in cm can be calculated by dividing this value through the material's density: $9.37\,cm$ for silicon, $0.33\,cm$ for gold and $1.21\,cm$ for tin. [4]

The thickness of a material is often expressed in the percentage of its radiation length. A $450\mu m$ thick silicon detector uses $0.48\%\,X_0$. A reduction in terms of radiation length is desired in order to minimize the particle track deflection. In particle detectors, a maximum radiation length of $0.1\%\,X_0$ per layer is mandantory.

[5] average length between collisions

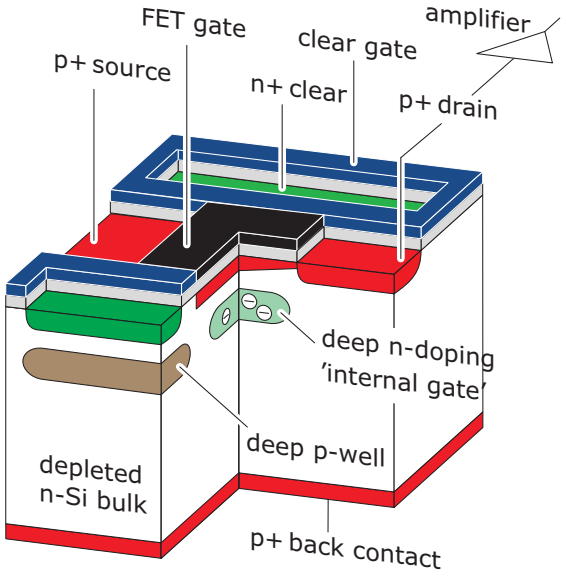

Figure 2.8: Sketch of a DEPFET with drain readout. [10]

2.3 The DEPFET Detector

The DEPFET detector is a monolithic active pixel sensor. In hybrid pixel detectors, the first amplification stage is located in an additional chip. However, a DEPFET has an amplification transistor integrated in every pixel. The extremely small input capacitance of this transistor allows a low noise amplification at room temperature. A fast and complete charge collection is made possible by the drift in a fully depleted bulk.

2.3.1 The DEPFET Principle

The DEPFET uses a pn-junction with a fully depleted bulk for signal generation and sidewards depletion to modulate the electrical field. A p-MOS signal amplification transistor is integrated in the front-side of the high resistivity n-type detector material. The highly p-doped back side implantation and the p-implantation of the transistor are used for sidewards depletion. The n^+-contact needed for depletion is not shown in figure 2.8 and is located outside the sensitive area. The potential minimum for electrons is shifted towards the front side, to $\approx 1\mu m$ below the surface. A structured n^+-implant is located beneath the transistor channel and creates the potential minimum, which collects the signal electrons.

Charged particles create electron-hole pairs in the fully depleted bulk. The holes drift towards the back side contact, while the electrons move to the front side and accumulate in the potential minimum below the transistor channel. The signal charge, stored in this deep n-implant, modulates the transistor channel and can be considered as an *internal*

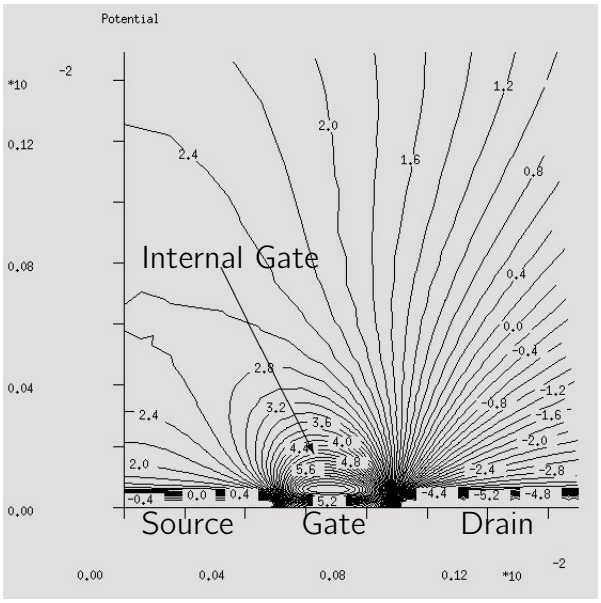

Figure 2.9: Equipotential lines of the electric field in the DEPFET detector bulk, showing the source-gate-drain region with the internal gate. [11]

gate. Figure 2.9 shows the equipotential lines of the electric field in the transistor region and the potential minimum of the internal gate. The change in transistor current dI is proportional to the change of signal charge dQ in the internal gate and defines the internal amplification g_q:

$$g_q = \frac{dI}{dQ}$$

The devices with a standard channel geometry show a g_q of approximately $400pA/e^-$. The electric field in the depleted region collects the charge in the internal gate within less than $60ns$ [10].

To read out the signal modulated by the internal gate, the DEPFET is switched on by the external gate of the transistor. As a readout is non-destructive, a DEPFET can be considered as an integrating device and can be read out multiple times without loosing signal information. The DEPFET transistor doesn't need to be switched on during signal collection, because the drift of signal charge into the internal gate is not influenced by the external gate. This allows a low power dissipating operation and makes an active cooling of a DEPFET detector obsolete.

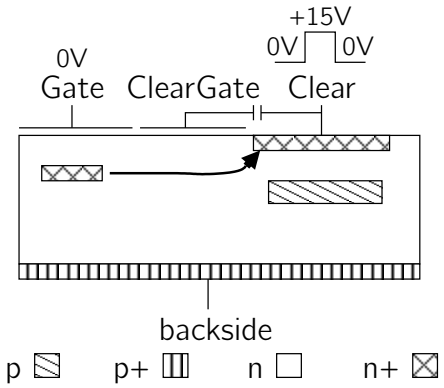

Figure 2.10: Charge removal from the internal gate by a clear pulse on the clear contact.

2.3.2 Charge removal

As the readout of the DEPFET is non-destructive, means of removing charge from the internal gate are necessary. The internal gate will fill up by either signal or thermally generated electrons (leakage). The sensor gets insensitive to new signal charge, if the internal gate is not cleared.

Figure 2.10 shows a cross section of the DEPFET transistor with a clear and a clear-gate structure. A highly doped n-type implantation is used as a potential minimum for electrons and as a electrical contact for the clear voltage. It is located near the internal gate. The charge stored in the internal gate is removed through applying a high positive voltage on the clear contact. The electrons in the internal gate are attracted by the high voltage, drift towards the clear contact and are then removed.

A complete charge removal is crucial, because remaining charge will contribute to the noise value of the detector. To lower the potential barrier between clear contact and internal gate, a *clear-gate* structure is introduced. It can be held at constant potential or can be pulsed. The pulsing may be realized by capacitively coupling the clear signal to the clear-gate structure using the parasitic capacitances of the layout.

Electrons generated by ionization drift in the depleted bulk along the electric field. They aren't exclusively attracted by the potential minimum of the internal gate, but also by the n^+ implantation of the clear contact. Charge drifting into the clear does not influence the transistor current and is lost. To avoid this incomplete charge collection, a p-type implantation is created underneath the clear contact. It provides a potential barrier for electrons and shields the clear contact. This assures a complete charge collection. Figure 2.11 shows the equipotential lines in a Clear-ClearGate-Gate region. The potential barrier shielding the clear contact is located at a depth of $18\mu m$.

The DEPFET is insensitive during a clear cycle, because signal charge drifting into the internal gate is immediately removed.

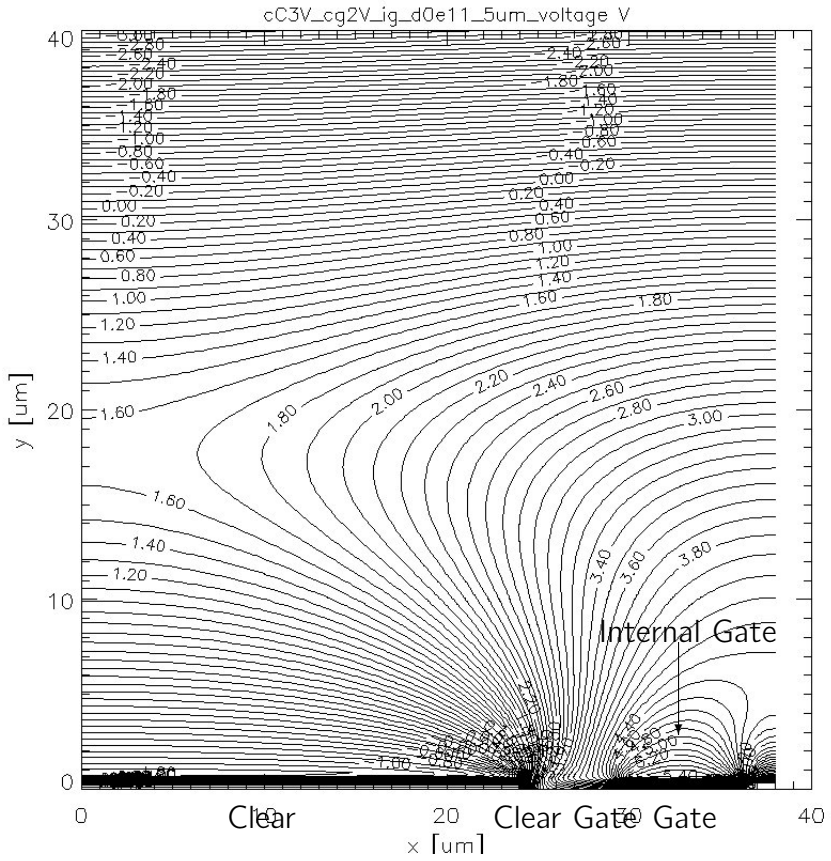

Figure 2.11: Equipotential lines of electric field in the DEPFET detector bulk showing a Clear-ClearGate-Gate region. [11]

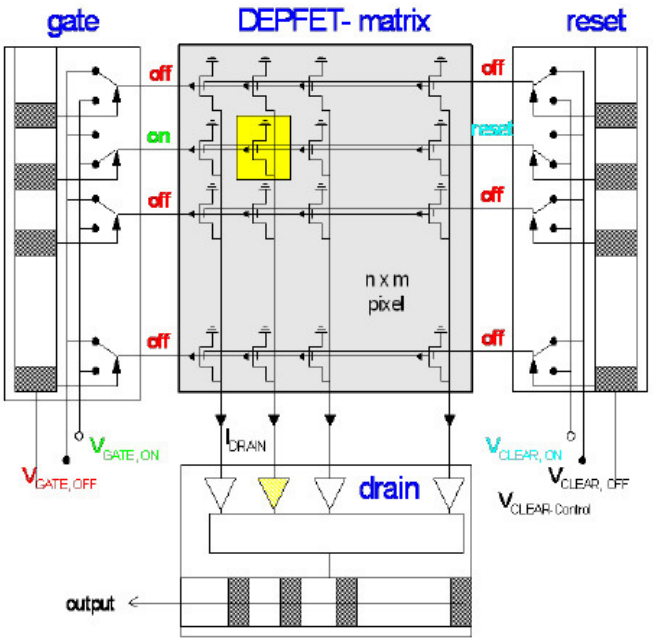

Figure 2.12: DEPFET matrix with current read out and steering of gate and clear signals. [10]

2.3.3 Building a Pixel Matrix

Single DEPFET cells are arranged regularly to build a pixel matrix. The clear and gate signals of the DEPFETs are connected row-wise and the drain signals are connected column-wise (see figure 2.12). The source voltage is distributed to all cells of the matrix (not shown in figure).

This connection scheme is possible, because the DEPFET is an integrating device and doesn't need to be read out continuously. For a continuous read out, every pixel would need it's own readout electronics, that lead to a high power dissipation. An active cooling would be required, but often is not possible in the space restricted area of the particle accelerators.

The matrix is read out row-wise. All transistors of a row are enabled by the common external gate signal. Signals, that are modulated by charge in the internal gate, can be read out by the electronics connected to the end of the drain lines. Clearing is also a row-wise operation. Two different readout modes exist:

double sampling After the signals of a row have been read out, internal gates are cleared and the row is re-read. The first read out value contains the signal and the baseline of the DEPFET cell. The second value contains only the baseline, if the clear has completely removed all charge. A baseline-free signal can be determined by subtracting the second from the first value.

single sampling The baseline of the matrix needs to be read out before any signal data is taken. It is stored for each pixel, to allow the subtraction of the baseline later on. They need to be updated regularly, as the baseline values of the matrix may change with time. Baseline compensation can be done in the readout chip, demanding on-chip memory to store the baseline values, or off-line in the analysis software.

Reducing the number of control signals, by grouping adjacent pixel rows, speeds up the frame readout. The number of drain lines has to be increased by the same factor, to read out the grouped rows in parallel. The data rate and the complexity of the readout electronics increases, but this also shortens the frame readout time.

2.3.4 System Noise

The noise of a system is a critical factor, as it influences its physics performance. A higher noise decreases the capability to detect low energy signals and lowers the spacial resolution of the detector. The noise value is often converted into *equivalent noise charge* (ENC), which describes the signal charge at the detector input needed to create the corresponding noise value. In case of the DEPFET, the ENC corresponds to the number of electrons in the internal gate.

$$ENC^2 = \frac{I^2}{g_q^2}$$

converts a current noise into ENC. Different processes are involved in the generation of noise in the DEPFET system:

Thermal noise is created by the thermally induced motion of charge carriers in a conductor.

Shot noise is a leakage current created by a random generation of electron-hole pairs in the sensor.

Flicker noise Charge trapped in the gate region influences the transistor current. The noise spectrum has a frequency dependence of $1/f$. Flicker noise is also called $1/f$ noise.

To limit the influence of $1/f$ noise, the bandwidth of the read-out circuit has to be limited at low frequencies. The $450\mu m$ thick devices shows a S/N > 110 [12].

2.3.5 Radiation Damage Effects

Radiation damage effects on the DEPFET transistor are mainly a shift of the threshold voltage, a build up of states at the interface between Si and SiO_2 and a reduction of the transconductance g_m.

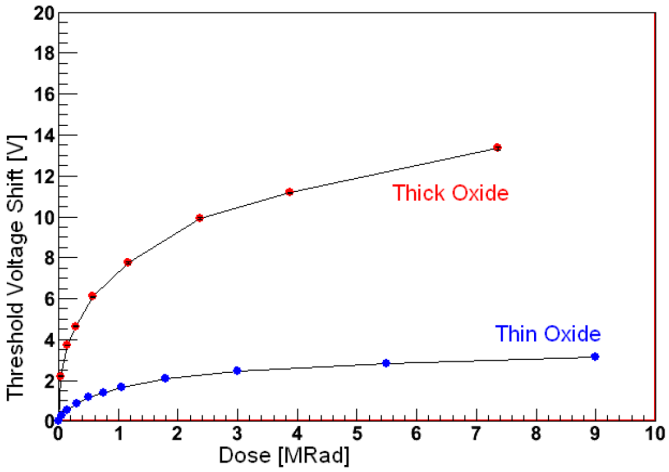

Figure 2.13: Threshold shift of a DEPFET transistor for 2 different gate oxide thicknesses after irradiation up to $9Mrad$. [13]

The DEPFET test-structures show a shift in threshold voltage of $\approx 13V$ after an irradiation of $7.5Mrad$ ionizing dose. The effects of ionizing radiation on the DEPFET can be reduced by a thinner gate oxide. However, the oxide thickness also affect other parameters like the internal amplification. Figure 2.13 shows the threshold voltage shift as a function of radiation dose for thick and thin oxides on DEPFET test-structures. The threshold shift has a great influence on building the system and can be reduced to $\approx 3V$ by using thinner oxides. All components need to be able to cope with this shift. The specially build power-supplies need to provide a wider voltage range and the steering chips have to be designed in a technology which is able to handle these voltages.

Radiation effects on the steering chip will be discussed in chapter 5. Irradiation results on the read-out chip DCDB are not available at the time of writing.

3 The DEPFET as a Vertex Detector

In high-energy physics, detector systems consist of many sub-detectors which are used to detect the interaction products. Typically, a calorimeter is used for energy measurements, a tracking device measures the particle momentum in a magnetic field and the vertex detector determines the primary interaction point and secondary decays.

A vertex detector is the innermost detector, located closest to the interaction point of the accelerated beams. It consists of several cylindrical layers of sensors surrounding the interaction point and should be a pixel detector (2-dimensional device) with a high spacial resolution. Their distance to the interaction point should be minimal in order to reconstruct a vertex with a high resolution, by extrapolating the hit points in the layers of the detectors.

3.1 The DEPFET Module Concept

The steering of the gate and clear signals and the digitalization of the charge information is done by specially designed silicon chips. To meet size, material budget, speed and noise goals, the chips have to be located close to the matrix. The chips can be directly connected to the matrix by wire- or bump-bond techniques or by an intermediate layer of PCB[1], silicon or a kapton based flex board. The control, data and power lines of all components of the detector system need to be interconnected and routed to a connection point. From there, a cable connects the system to the data acquisition (DAQ) and power supplies. This assembly of detector, steering and read out chips, routing and outside connection is called a module.

Figure 3.1 shows a photograph of the hybrid PCB 'S3A' with the 2 *Switcher-2B* steering chips at the left and the right of the DEPFET matrix. The readout chip *Curo* is located below the matrix. The hybrid PCBs are used for testing and characterization of the DEPFET matrix and the chips. A FPGA board is connected to this PCB, which communicates with the PC, configures and controls the chips and transfers the digitized DEPFET signal data to the software.

Using PCBs to build a detector system is the first step, but often a PCB cannot be integrated into a particle accelerator. The space available for a vertex detector module,

[1] **P**rinted **C**ircuit **B**oard

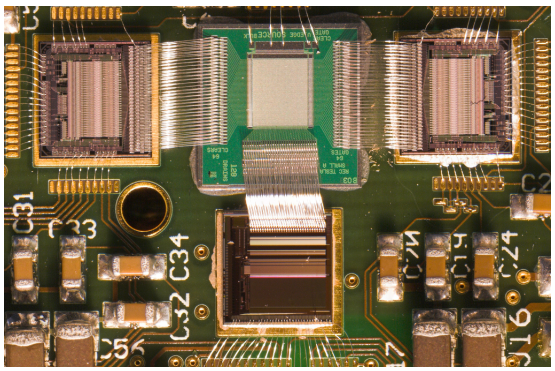

Figure 3.1: Switcher-2B steering chips, matrix and Curo readout chip on 'S3A' hybrid PCB. [14]

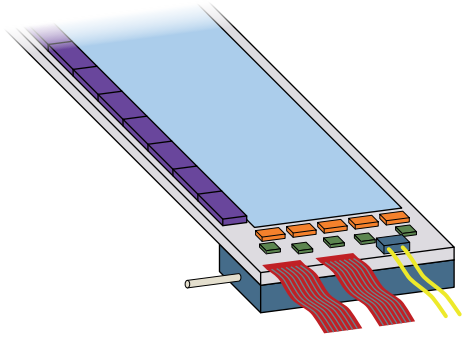

Figure 3.2: Futuristic sketch of a DEPFET module. [15]

located close to the interaction point of the particle accelerator, is minimal. The thickness of the PCB material and its components is enlarging the radius, increasing multiple scattering and deteriorating the physics performance of the detectors. A thin and small solution is needed.

The All-Silicon Model

By enlarging the silicon size of a DEPFET sensor, while keeping the size of the active area constant, space can be created for directly mounting the steering and readout chips onto the detector silicon and for routing the interconnection and power traces. On a highly integrated and densely populated area of such all-silicon modules, the routing of a huge amount of signal and power connections is a difficult task. The components, located on the detector silicon, must not influence the detector or the electronics operation.

Figure 3.2 shows a sketch of the module concept. The steering chips are located on the long side of the detector, while the readout chips are mounted on the short end. This setup results in short and low capacitance matrix steering signals, which can be charged

quickly. A high capacitive load on the drain lines is not as limiting as on the control lines, because the DEPFET is operated in drain read-out mode, yielding to a current signal.

Control, data and power lines have to be connected directly to the silicon, the module is mounted on a support structure, which is also used for actively cooling the readout chips. By thinning the silicon of the detector and the chips, the material budget of the module can be reduced furthermore. For interconnecting the chips with the detector module, the flip chip technology has been chosen. Details on interconnection will be presented in chapter 6.

Cooling

The integrated circuits, the leakage current of the detector and the currents flowing in signal and power traces are heat sources, that often need to be actively cooled. With increasing temperature, the module expands and the pixel positions of the detector change relative to the accelerator's interaction point. This influences particle track reconstruction negatively. Another effect is thermal runaway, where an increasing temperature increases the leakage current, which itself generates more heat. But cooling of an inner layer detector, surrounded by many more detectors, is not easy, as the area for installing the module's cooling is confined. The pipes for the cooling medium and the means of heat transfer must not significantly increase the material budget of the active volume. In the closed volume of the pixel detector the heat cannot escape and the temperature will rise. The heat has to be actively removed, because air cooling in detectors with a high power density is not sufficient. Therefore, cold liquid or gas has to be used to remove the heat close to the source.

The modules have to be supported by a stable mechanical mounting solution, which also has to be minimized in terms of material budget. The mounting structure can also be used as a cooling element, because the modules can transfer heat directly to it.

3.2 Wafer Thinning

The multiple scattering effect, that influences a particle's track while passing through matter, should be minimized. It lowers the impact parameter resolution for low energetic tracks. However, thinning the sensor material is not only improving the material budget, but also is decreasing the detector's signal-to-noise ratio.

Thinning silicon devices on wafer level is a commercially established process, where the unused back side of the device is removed by mechanically lapping and chemically etching. The DEPFET technology needs a back side implantation for a complete depletion of the sensor's volume. Processing the back side implantation after thinning the device to less than $100\mu m$ is difficult, because the thin silicon foil might be damaged. A different

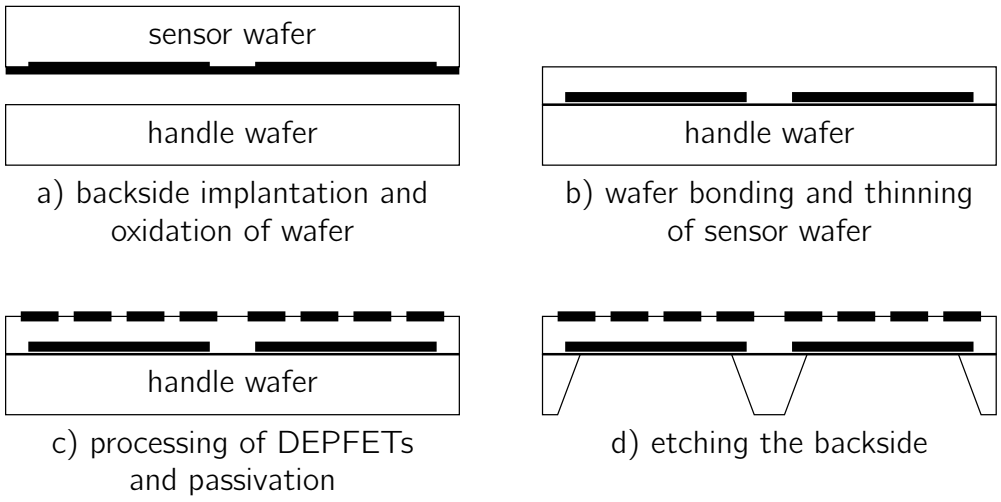

Figure 3.3: Thinning steps of back side processed DEPFET sensor wafers.

thinning technology has been developed at the MPI Semiconductor Laboratory in Munich, where the DEPFET structures are completely processed before the thinning is applied.

Figure 3.3 illustrates the thinning process. First, the back side is processed on a high grade sensor wafer and then oxidized (a). The back side of this wafer is then bonded by direct wafer bonding to a handling wafer and the sensor wafer is thinned to the desired thickness by CMP[2] (b). The DEPFET structures are processed on the thinned sensor wafer (c). Afterwards, the thinning mask is applied to the handling wafer and the silicon is removed by anisotropic etching, which stops at the oxidized layer (d).

The support frame of the module is needed to mechanically support the thin active area and carry the steering chips. It allows to build a thin all-silicon module without glueing the thin silicon onto a support structure. Different temperature coefficients of silicon and support material could cause problems, which can be avoided in an all-silicon approach. The silicon support frame is partially thinned to further reduce the material budget of the detector. Figure 3.4 displays a hole pattern etched into the frame, which reduces the material by 33%. The thinned material is less stiff and a gravitational sag of 20μ along the long side of the module has been observed [16]. The support frame makes the module stiff enough to be handled by hand. Figure 3.5 shows a module with a size of $10cm \times 1.3cm$, where the active area is thinned down to $50\mu m$. The support frame is 450μ thick and thinned with the presented hole pattern. In figure 3.6 is a side view of a thin module with an attached steering chip shown.

[2] **C**hemical **M**echanical **P**olishing

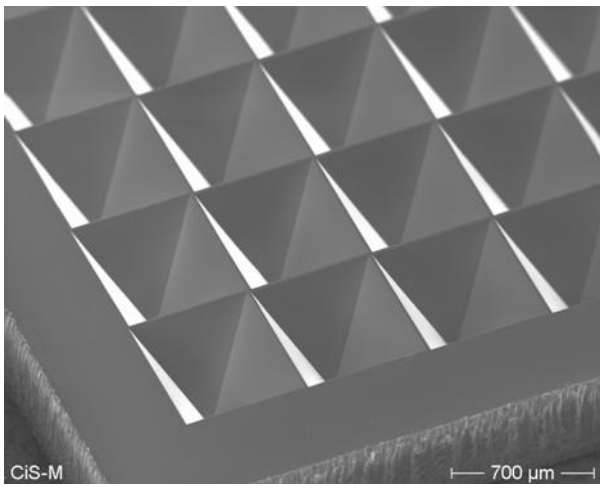

Figure 3.4: Photograph of the hole pattern of the thinned balcony. [12]

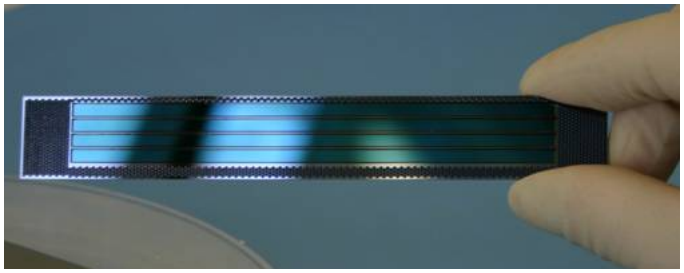

Figure 3.5: Photograph of a $10cm \times 1.3cm$ mechanical sample with a thin active area and a hole pattern in the support frame. [17]

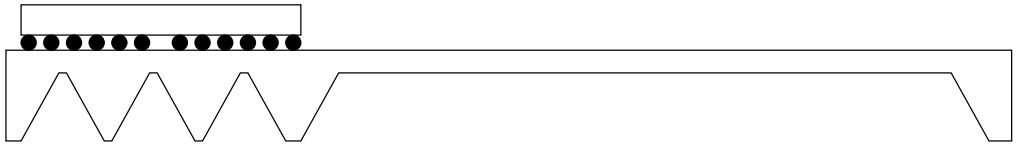

Figure 3.6: Schematic side view of a thin module with a hole pattern in the support frame and a steering chip attached by bump bonding.

3.3 The International Linear Collider

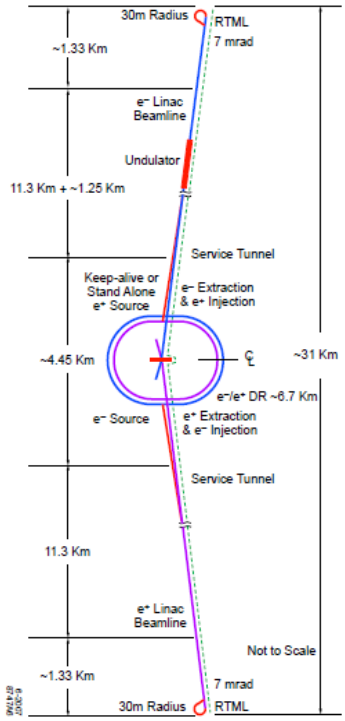

Figure 3.7: Schematic layout of the ILC linear accelerator. [18]

The currently running Large Hadron Collider (LHC) at CERN is a proton-proton collider with center-of-mass energies of up to $14TeV$ and a luminosity (a measure of collision rate) of up to $10^{34}cm^{-2}s^{-1}$. It is currently running with energies of $7TeV$ and a luminosity of $10^{32}cm^{-2}s^{-1}$. Physicists were able to validate aspects of the Standard Model of particles and forces [19]. New Physics beyond the Standard Model might be discovered with this collider. The discoveries made should be enhanced with more precise measurements. A hadron collider can't provide this precision, as it is limited by the uncertainty of the interaction's initial energy. A lepton collider is needed, as lepton collisions have a well defined initial state and all of their center-of-mass energy is available at the primary collision. The ILC is planned to provide this high precision by electrons colliding with positrons at energies between $90GeV$ and $1TeV$.

Two major concepts of building the accelerating part of a collider exist: the circular and the linear approach. In a circular collider, particles are accelerated in a ring and are gaining energy in every turn. They are brought to collision after reaching their target energy. The particles are loosing energy by synchrotron radiation, which is emitted when they are forced on a circular path. This energy loss is proportional to $1/m^4$ and is significant at high energies for light particles like electrons. Therefore, the concept of **lin**ear **ac**celeration (linac) is introduced. The particles start at two different places, are accelerated on a straight line and are brought to collision. In circular accelerators, the particles are accelerated at one segment of the circle and reach the target energy after multiple circulations. A linear accelerator has to reach the target energy by a single passage. The particle is accelerated among the full length of the beam line. Figure 3.7 shows the low energy damping rings with $6.7km$ circumference in the middle, from which the particles are fed to the ends of the two main linacs. From there, they are linearly accelerated on a length on $\approx 11km$ per side. Prior to the collision in the interaction point in the middle, the beams are focused to a size of $639nm \times 5.7nm$.

The ILC uses the superconducting technology to accelerate the particles. 16000 RF cavities are installed and operated at $1.3GHz$ with an accelerating gradient of $31.5MV/m$ per cavity. They are build of niobium instead of copper, which has a factor of 10^6 lower surface resistance. This leads to a much lower power consumption, even if the energy needed for cooling to superconducting temperature is taken into account. An electrical power of $230MW$ is required to reach the luminosity of $2\times10^{34}cm^{-2}s^{-1}$. The accelerator

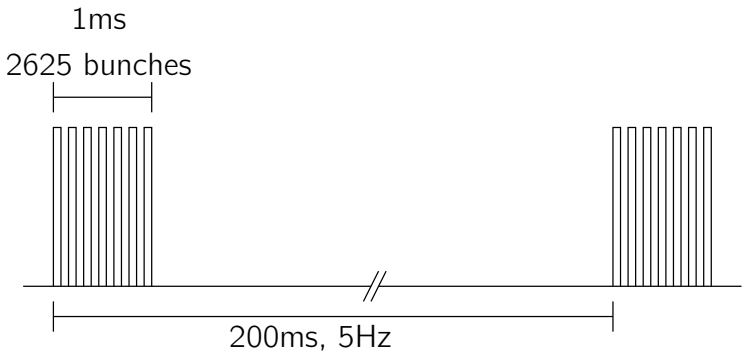

Figure 3.8: ILC beam timing with 2625 bunches within 1ms and 199 ms pause.

has a repetition rate of $5Hz$ with a beam pulse length of $1ms$ and a $199ms$ pause (see figure 3.8). The $1ms$ beam pulse contains 2625 bunches with 2×10^{10} particles per bunch, resulting in an average beam current per pulse of $9mA$. An accelerator length of 31km is mandatory to reach a center of mass energy of $500GeV$. The length has to be extended to reach $1TeV$. [18]

However, neither the decision to build the ILC has been made, nor where to build it. Governments in the US and the UK are forced to cut the budget for research and development. The US reduced its funds to a fourth[20], the UK research budgets were cut severely[21]. Thus, the development of the ILC has been slowed down.

The large delay of the ILC made the search for an intermediate application for the DEPFET detector necessary. The development of a vertex detector based on the DEPFET technology was continued for the Belle detector at the SuperKEKB accelerator facility in Japan.

3.3.1 Vertex Detector Geometry for ILC

Reconstruction of all tracks and the assignment of the vertices to the primary, secondary and tertiary events requires a high resolution detector with a spacial resolution of $4\mu m$. Multiple layers of detectors are placed around the beam pipe with a small overlap for a precise track reconstruction.

The DEPFET uses pixel sizes of $25\mu m \times 25\mu m$, which allows a binary resolution of $25\mu m/\sqrt{12} \approx 7\mu m$. The pixel signal is compared with a threshold value to detect a hit at the binary read-out scheme. Only this hit information is stored. A resolution of $3.5\mu m$ is achieved with the $50\mu m$ thin detector by interpolation using the center-of-gravity method and a signal-to-noise ratio of 40 [12].

Figure 3.9 shows the innermost layer. The modules are placed as close as possible to the beam pipe, at a radius of $1.5cm$. The steering chips are at the long side of the matrix and the readout chips are at the short end. The modules are overlapping, to

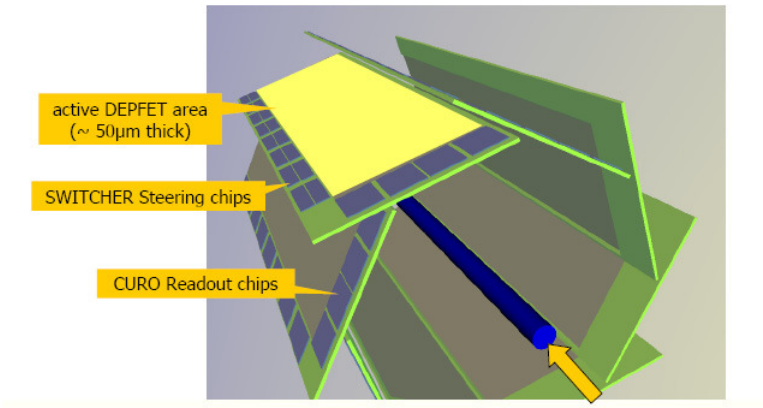

Figure 3.9: ILC inner layer modules placed around the beam pipe with steering and readout chips. [12]

Layer	Radius (mm)	Number of ladders	Ladder length (mm)	Ladder width (mm)	Frame Rate
1	15.5	8	100	13	$50\mu s$
2	26	8	2x125	22	$250\mu s$
3	38	12	2x125	22	$250\mu s$
4	49	16	2x125	22	$250\mu s$
5	60	20	2x125	22	$250\mu s$

Table 3.1: Proposed ILC DEPFET vertex detector layer configuration. [12]

cover the inactive balcony of one module by the active area of the next module. The detector's active area has a size of 4096×512 pixels, with a length of $\approx 10cm$, given by the beam pipe, and the pixel size of $25\mu m \times 25\mu m$. Table 3.1 shows the proposed geometric properties of the 5 layers of the vertex detector.

3.3.2 Read-out and Timing

As the detectors are in a high multiplicity environment, where many events occur simultaneously, many pixels are hit by incident particles. With the given accelerator timing parameters and physics simulations, the hit multiplicity is ≈ 0.05 hits per mm^2 and bunch for the inner layer. Assuming that, due to charge sharing, 30% of the particles create hits not only in one but two pixels, the integrated occupancy in one bunch train would be 15%. This amount of hit pixels per read out frame complicates track reconstruction and is unacceptable. The occupancy has to be reduced to 1% by reading out the detector several times during a bunch train. The readout speed is the driving force in the detector development for the ILC. [12]

Reading a 4096 row matrix requires high speed steering and readout chips with low noise

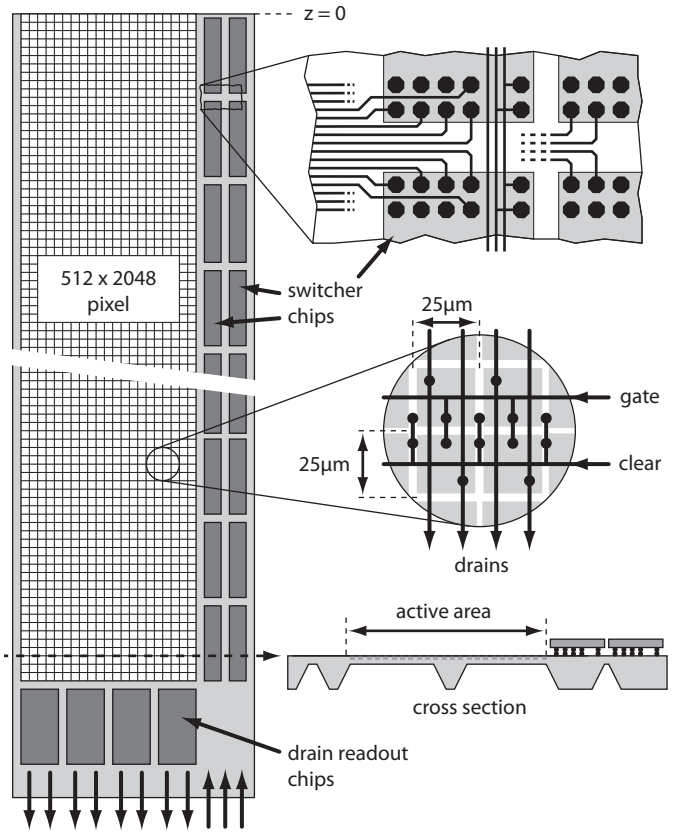

Figure 3.10: ILC half module drawing with cross section of the thinning, double row organization and chip location. [22]

and low power consumption. A trade-off between speed, noise and power consumption needs to be found. The effective readout rate can be doubled by splitting the matrix in 2 halves and reading out from both ends. The electronics are running at moderate speed with low noise and without excessive power consumption. To reduce the speed even more, two consecutive rows are grouped and controlled by the same gate and clear signals (see figure 3.10). This requires twice the amount of drain lines and readout electronics. The matrix of the inner layer with 4096×512 pixels would then connect to 1024 channels with gate and clear signals and 1024 readout channels per half module.

The occupancy can be reduced when reading out with an effective row rate of $40MHz$, with both halves of the matrix running at $20MHz$. Because a sample-clear-sample (double-sampling) readout was chosen for the ILC, the sampling and digitalization of two values had to be within $50ns = 1/20MHz$ per double row. Therefore, the ADCs digitizing the analog DEPFET values have to run with $40MHz$. One frame is read out in $\approx 50\mu s$. 20 frames can be read out in a bunch train of $1ms$.

The occupancy of layers 2-5 is much lower, because the distance to the interaction point is greater. This allows larger detectors and a slower readout speed of $250\mu s$ per frame.

Layer	Number of ladders	Active pixels	Power per ladder	Power per layer	Average
1	8	2048	12W	96W	
2	8	3072	21W	168W	
3	12	3072	21W	252W	
4	16	3072	21W	336W	
5	20	3072	21W	420W	
total				1272W	6.4W

Table 3.2: ILC DEPFET power consumption during burst and averaged to the 200ms beam timing. [12]

The steering signals are controlled by the Switcher-3 chip (see chapter 5.1). One chip is needed for the clear and another for the gate signals, as each chip supports only one steering voltage. Two columns of chips are located on the balcony.

A drain current digitization with the Curo chip was foreseen (chapter 3.5.1). The high capacitance of the long ILC matrixes caused an unacceptable noise contribution by the Curo. A successor chip called DCD (see chapter 4.1) had to be developed.

3.3.3 Module Power Consumption

A benefit of the DEPFET is its low power consumption. A pixel consumes $I_D \times V_{DS} = \sim 100\mu A \times \sim 5V \approx 500\mu W$ during read out. The power consumption of a switched off pixel is almost zero, although it is still sensitive and collects signal electrons. A half module has 2 rows of 512 DEPFET pixels activated during read out with the readout scheme described above. Therefore, an inner layer module consumes 1W. Adding the Switcher steering chips' $0.85W$ and the DCD readout chips' 2048 channels, with $5mW$ per channel, this sums up to $\approx 12W$.

Table 3.2 shows the approximative power consumption of all layers. The total power consumption of $1272W$ during reading breaks down to $6.4W$, because the DEPFETs and the electronics are only active and read out during the bunch train of $1ms$. The system is idle in the $199ms$ pause. Since most of the power is dissipated by the readout chips located outside the acceptance region, an active cooling is feasible without adding material to the critical active area. The power dissipated in the active volume by the DEPFETs and the steering chips is low and can be removed by air cooling. [12]

3.3.4 Irradiation Damages and Radiation Length

An expected dose of 200krad of ionizing radiation and $10^{11} n/cm^2$ 1MeV neutron equivalents will be deposited in the silicon devices close to the interaction point during 5 years

of ILC operation. The influence on the DEPFETs from PXD4 production was tested by irradiation up to a dose of 900krad with gamma rays and $3x10^{12}n/cm^2$ 1MeV neutron equivalent protons, which simulates 30 years of operation. Bulk damages, with change of the effective doping concentration, are not observed for non-ionizing radiation, as expected. A by $2e^-$ ENC slightly increased noise at higher temperature indicates an additional shot noise. [12]

The radiation length of the module should be about 0.1% in order to reduce multiple scattering effects. The material budget would be already used up by a $100\mu m$ thick sensor, without taking the additional radiation length of steering chips and interconnection technology into account. The readout chips are not added, because they are outside of the detector's acceptance area. To meet the requirements, the $450\mu m$ thick silicon substrate of the DEPFET detector has to be thinned to $\approx 50\mu m$. It is only partly thinned for stability reasons and mainly in the active region. A signal to noise ratio of >40 can be achieved due to the good properties of the DEPFET, even with the $50\mu m$ thin active area. The thin active area and the support frame add 0.1% X_0, where the also thinned steering chips will add another 0.01%. As the chips are connected with a flip chip technology using gold bumps, the material added by the gold has to be included in the material budget. It adds another 0.01%. The radiation length sums up to an acceptable value of 0.12% X_0. [12]

3.3.5 Alternative Detector Concepts

Several other detector concepts have been proposed for the ILC pixel vertex detector. The use of Charge Coupled Devices with a column parallel read-out to improve speed or with an in-pixel storage are options, together with monolithic active pixel sensors based on CMOS technologies.

Charge Coupled Devices

Charge Coupled Devices (CCD) for the ILC can have pixel sizes down to $2 \times 2\mu m^2$, but a pixel size of $20 \times 20\mu m^2$ is sufficient to achieve the required resolution. The pixel detector consist of five layers mounted in a low-mass foam cryostat. The inner layer modules are $100 \times 13mm^2$ large and are read out from both ends, while the four outer layers consist of $125 \times 22mm^2$ large devices. Two of each are glued together to form the ladder. The sensitive epitaxial layer is $20\mu m$ thin, which allows the detector to be thinned close to this value for a low material budget. A low read-out noise of 10 e^-ENC gives a good S/N, even with thin devices. Fully depleted devices are mandatory to collect the charge within a clock cycle. A point resolution of $5.8\mu m$ can be achieved. Charge sharing between pixels is not available and the resolution cannot be increased by interpolation.

Charge trapping due to irradiation damages could cause signal electrons to be trapped

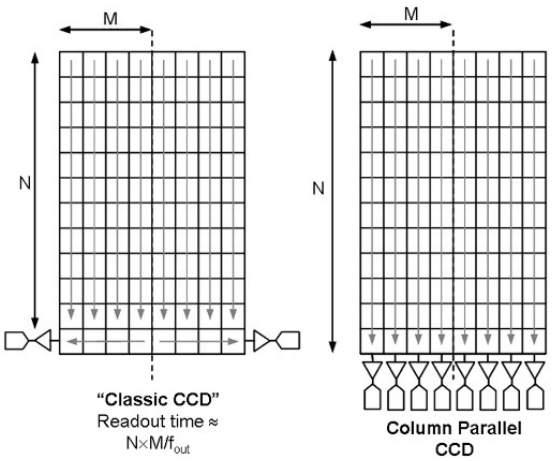

Figure 3.11: Comparison of standard and column-parallel CCD read-out. [23]

while they are traveling from their generation point to the output. The high capacitive load of clock signals, connected to every pixel and used for charge shifting, cause high power dissipation. Low swing signals of 2V are used in contrast to the 10-15V of standard designs. The capacitance of a detector area of $10cm^2$ sums up to $50nF$ and even with the reduced swing is a current of $\approx 10A$ needed when operated at $50MHz$. The output drivers designed in the CCD-technology need a high supply voltage in the range of 15-20V and cause a high power dissipation. CMOS circuits can't be integrated due to incompatible technologies.

A column-parallel readout is used to increase the read-out speed. Figure 3.11 illustrates the differences between standard and parallel read-out. A separate processing chain is used for every column. The read-out chip is flip-chip bonded to the detector with 125 solder bumps. It allows a constant 20kHz frame rate and is operated at 50MHz on the inner layer to reduce the occupancy to acceptable limits. It features double sampling, a 5-bit ADC and a read-out FIFO with 132 entries. [24][23]

Charge Coupled Devices - In Pixel Storage (ISIS)

As sensors are sensitive to Radio Frequency pickup caused by the accelerator during charge to voltage conversion, a new concept of CCD has been proposed. Figure 3.12 shows the in-situ storage (ISIS) of 20 charge signals in a CCD pixel. During the 1ms bunch train, the charge is shifted from the photo-gate to the storage pixels with a moderate frequency of 20kHz. The stored signals are read out during the inter-bunch pause of 199ms with a frequency of 1MHz. This is by a factor of 50 slower than the continuous column-parallel CCD read-out. [24]

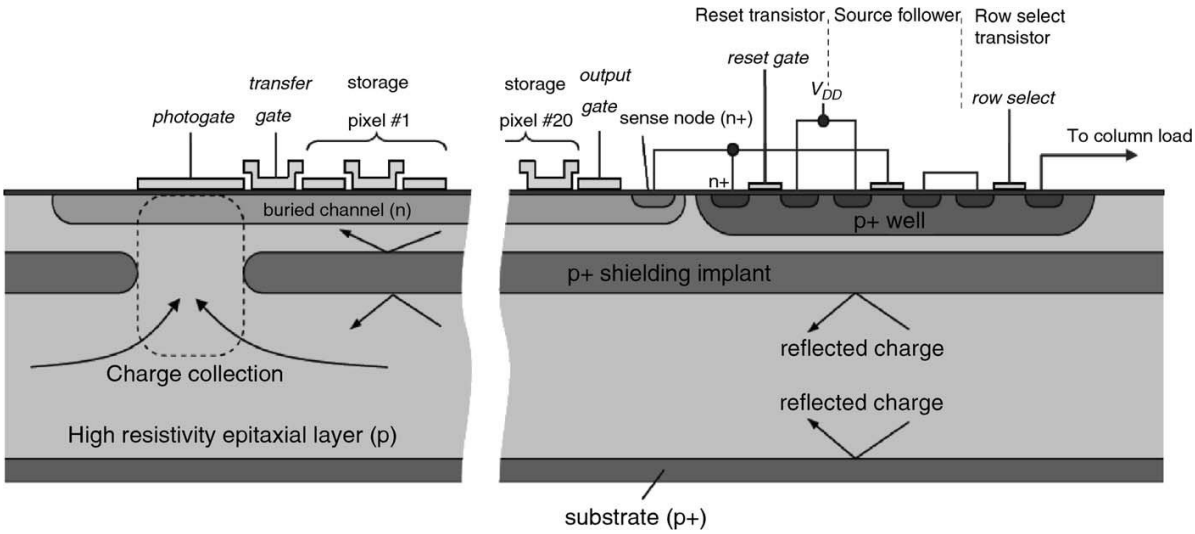

Figure 3.12: Cross section of CCD with in-situ storage. [24]

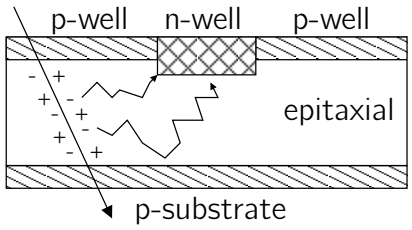

Figure 3.13: Detection principle of a CMOS sensor. Generated signal charge is traveling by thermal diffusion to the collection electrode.

Monolithic Active Pixel Sensors

In monolithic active pixel sensors, signal processing electronics are integrated on the sensor substrate. A double-well CMOS process with a $5 - 15\mu m$ thin epitaxial layer is used. The signal charge is generated by the incident particle in the epitaxial layer and is collected in a diode formed by a n-well implantation in the p-epi layer (figure 3.13). Since no electrical field is available, like in a fully depleted bulk, the signal electrons travel by thermal diffusion into the collection electrode. The thermal diffusion leads to a larger signal collection time of $\approx 100ns$. A thinner epitaxial layer leads to shorter collection times and smaller charge spreading, but also to a smaller signal. A S/N of 20-30 and a point resolution of $1.5 - 2.5\mu m$ was achieved with $20\mu m$ epi layer thickness.

A read-out time of $\leq 25\mu s$ is required to keep the occupancy below 1%. The pixel columns are organized perpendicular to the beam axis and are read out in parallel in order to achieve a shorter column read-out time. The charge is digitized with a 4-5bit ADC integrated in each column. Depending on the layer, a pixel pitch ranging from 20 to $40\mu m$ is used. The CMOS process allows integration of circuits for amplification, pedestal correction, digitization, etc in every pixel. Detector thinning to a few tens of microns is permitted by the thin active volume of the epi layer. Thinning to $20\mu m$ is currently evaluated. [25]

3.4 The Belle II Experiment at SuperKEKB

Since the deployment of the ILC has been delayed, a new application for the DEPFET pixel vertex detector was found in the next generation B-factory experiment located at the National Laboratory for High Energy Physics (KEK) in Japan. The Belle II detector is an upgrade of the Belle detector, which is installed at the KEKB accelerator. Together with the detector, the accelerator will be upgraded too and will be called SuperKEKB. A central part of the new Belle II detector will be the two layers of DEPFET pixel vertex detectors.

The Belle II detector will be used to study details on New Physics processes beyond the Standard Model, which are expected to be uncovered at hadron colliders in the next years. Many fundamental processes in the Standard Model of interactions remain unanswered. Upgrading the KEKB accelerator to a Super-B factory allows new measurements in heavy flavor physics and helps to point out the deviations from the Standard Model.

Pairs of B and anti-B mesons are generated by colliding electrons with positrons, which decay with different patterns. This difference is called *charge-parity (CP) symmetry violation*. An example of CP violation is the dominance of matter in the universe. Matter and anti-matter should have been created by equal parts during the Big Bang. The CP violation is a necessary condition to create the matter-antimatter asymmetry, but this behavior cannot be predicted accurately with the Standard Model.

The Belle experiment at the KEKB accelerator found extremely rare B decays called electroweak penguin mode, but not enough events were found to be really sure. An upgrade of the Belle detector and the accelerator should help to observe more of these extremely rare events.

3.4.1 Accelerator Upgrade

The current KEKB accelerator holds the world record of the collider with the highest luminosity. After the upgrade to SuperKEKB, the luminosity will be increased furthermore by a factor of 40 to $8 \times 10^{35} cm^{-2} s^{-1}$. Compared to the ILC, the SuperKEKB has a 40 times higher luminosity, but a 50 times smaller center of mass energy of $10 GeV$. They both are electron positron colliders, but the SuperKEKB is using the double-ring collider technology. This is feasible due to the much lower particle energies.

Figure 3.14 shows the two rings with a circumference of 3km. One ring is the high energy ring (HER) for electrons accelerated to an energy of $7 GeV$, the other is the low energy ring (LER) for positrons, with an energy of $4 GeV$ [10]. Electrons are generated in an electron gun and accelerated in a linear accelerator for injection in the HER. A tungsten target is inserted into the linac to generate positrons, which are then fed into the LER.

A higher beam current together with a good focusing of the beams at the interaction point is needed to increase the luminosity. The electromagnetic beam-beam interactions

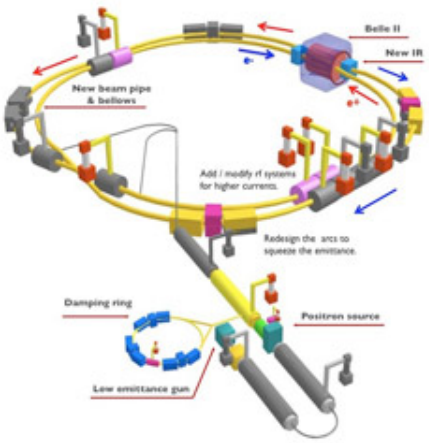

Figure 3.14: Schematic view of SuperKEKB accelerator. [26]

need to be decreased as well. A negative effect is caused by the electron clouds generated in the beam pipe by synchrotron radiation. The radiation hits the pipe's walls and kicks out electrons. These free electrons can have enough energy to create secondary electrons themselves and are disrupting the positron beam.

A high luminosity also influences the detectors, especially the pixel vertex detector. It is located the closest to the interaction point and needs to be read out very fast in order to cope with the extremely high hit rates and to keep the occupancy low. The occupancy is caused by beam-induced background radiation by the high amount of particles. Several interactions contribute [27]:

Beam-Gas scattering Beam particles change their momentum when they hit residual gas in the beam pipe. The momentum does not fit the B-field and the ring radius, causing the particles to hit the beam pipe walls and to create electron showers. This contributes the most to beam background radiation.

Touschek scattering is an intra-bunch scattering, which is proportional to the bunch current and number. It is inversely proportional to beam size and energy.

Synchrotron radiation is generated when fast moving particles are deflected by a magnetic field. This happens when the beam is forced to move on a curved path. A source is also the final focusing magnet, located close to the interaction region.

Backscattering from synchrotron radiation A strong magnet used for separating the two beams on the exit of the interaction region creates strong synchrotron radiation. This radiation hits a chamber $\approx 9m$ away and is backscattered into the interaction region.

Two options to achieve the high luminosity have been discussed by the accelerator developers: the high current option and the nanobeam option.

High Current Option

The high current option to increase the luminosity uses a higher beam current and optimizes the beam-beam parameter. A current of $9.4A$ in the low energy ring and $4.1A$ in the high energy ring was foreseen. Crab cavities were added to the accelerator to rotate particle bunches. The particle beams cross at the interaction point at an elevated angle (crab crossing) and the beams collide head-on, increasing the luminosity. But with the high currents of SuperKEKB, the crab crossing did not perform as simulated. Other problems arose with the high current option too: The synchrotron radiation stretched the bunches in the positron ring, which decreased the luminosity. The beam shape was different than designed, because of large magnet sizes at the interaction point, which also resulted in a luminosity drop. [26]

Nano Beam Option

Another approach was to decrease the beam size to a nanometer scale and to use a large crossing angle to reduce the longitudinal overlap of the two beams, instead of increasing the beam intensity. The smaller overlap limits the beam emittance, which is inverse proportional to the luminosity. The currents in both beams are about half of the high current option ($3.6A$ in the LER and $2.6A$ in the HER). A lower power consumption and thus a more economical machine can be build, without loosing the luminosity goals. The beam size of $\approx 10\mu m$ in horizontal and $\approx 60nm$ in vertical direction is achieved by superconducting magnets in the interaction region, which squeeze the beam to the nanometer scale. The nanobeam option was chosen to be built. [10]

3.4.2 Vertex Detector Geometry

With the nanobeam option of Belle II, the radius of the beam pipe is only 10mm, which allows a close mounting of the pixel detector and a good physics performance. But the low distance from the interaction point also increases the beam related background influence on the sensors, which is proportional to the inverse square of the radius. The high background induces a high occupancy of the detectors, which makes the use of strip detectors impossible. A pixel detector has a lower occupancy, because of the higher number of channels. Strip detectors can be used at radii larger than 40mm.

The PXD in the Belle detector consists of 2 layers of DEPFET ladders. They are based on the ILC development with extensions for the Belle II experiment. Figure 3.15 shows a drawing of the two barrels without the steering and readout chips. The ladders of both layers are 15.4mm wide, while the outer layer has much longer ladders. Overlapping ladders cover the inactive part of the support frame carrying the steering chips. The active area will be thinned to $75\mu m$ using the technology presented in chapter 3.2 to reduce the multiple scattering effects. The support frame is $400\mu m$ thick and will be

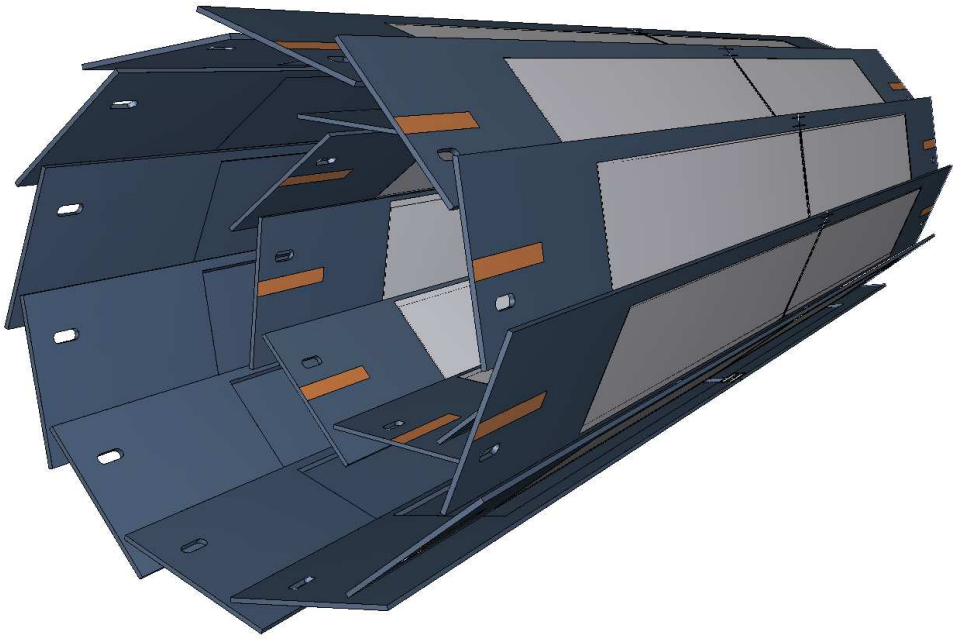

Figure 3.15: The two layers of Belle II PXD with the longer outer layer. The gray area marks the active region containing the DEPFET pixel cells. [10]

Layer	**Radius (mm)**	**Number of ladders**	**Length (mm)**	**Ladder active length(mm)**	**Pixel size** μm^2
1	14	8	2×68	2×45	50×55 and 50×60
2	22	12	2×85	2×62	50×70 and 50×85

Table 3.3: Belle II DEPFET vertex detector layer configuration.

partially thinned. The $75\mu m$ thin active area is mechanically more robust and allows better position resolution than the $50\mu m$ option. Charge generated by an incident particle passing through the thicker detector is shared between more pixels. [28]

Table 3.3 shows a summary of the ladder dimensions. The width of the modules is $15.4mm$ with a $2.2mm$ wide balcony for the steering chips on one side and a $400\mu m$ wide support frame on the other side of the module. The active area has a width of $12.8mm$. 256 pixel columns can be realized with the given pixel width of $50\mu m$. Both layers will have 1600 pixel rows with two different pixel pitches. Smaller pixels are located close to the beam collision point, while larger pixels are used towards the end of stave. The outer layer is build with $70\mu m$ and $85\mu m$ long pixels, whereas $55\mu m$ and $60\mu m$ short pixels are used on the inner layer [29] to keep the occupancy low.

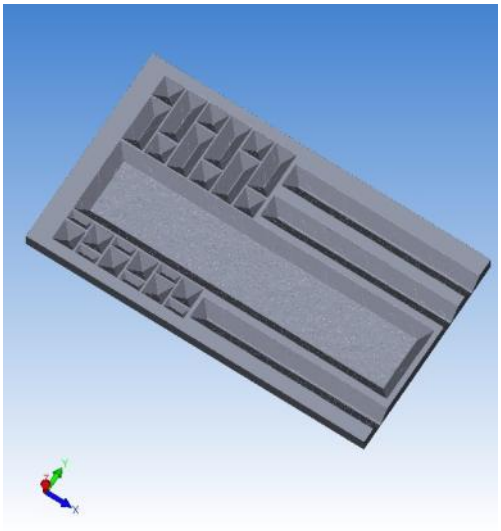

Figure 3.16: Etching simulation of thinned active area with frame perforation and notches for glueing two modules together. [10]

The ladders consist of two sensor modules glued together. This is necessary because the DEPFET technology's wafer size is limiting the length. Although the inner layer ladders would fit on a 150mm wafer, they are split too. This is necessary to increase the module's yield. Triangular ceramic pins are glued into grooves at the end of the module frame to get a rigid mechanical connection between two half modules (see figure 3.16). The notches are created by etching during the thinning process. No additional processing is needed.

23mm are foreseen at the end of each module for flip-chip mounting the readout chips to the ladder and to affix the ladder to a support structure by screws. The electrical connection of the modules, a multilayer kapton flex cable, will be mounted in this area, too. It consists of 3 layers of copper traces. The power supplies are routed on the top and bottom layers to build a defined environment for the high speed signal traces on the middle layer.

Figure 3.17 shows the mounting scheme with the beam pipe in the middle and two half barrels containing both layers. The outer layer is mounted on the support structure with the chips facing outwards and the inner layer facing towards the beam pipe. The support structure itself is mounted on the beam pipe, while one end is fixed and the other end floats on the beam pipe to compensate for thermal expansion. The ladders float on the structure using a slot instead of a hole for screwing the silicon to the structure. The kapton flex cable of 6mm width is affixed on the support structure for stress relief and to keep the electrical connection from the kapton to the silicon module stable. Between the kapton cables are the pipes for the coolant connected to the support structure. After everything is assembled on the two halves, they are mounted on the beam pipe.

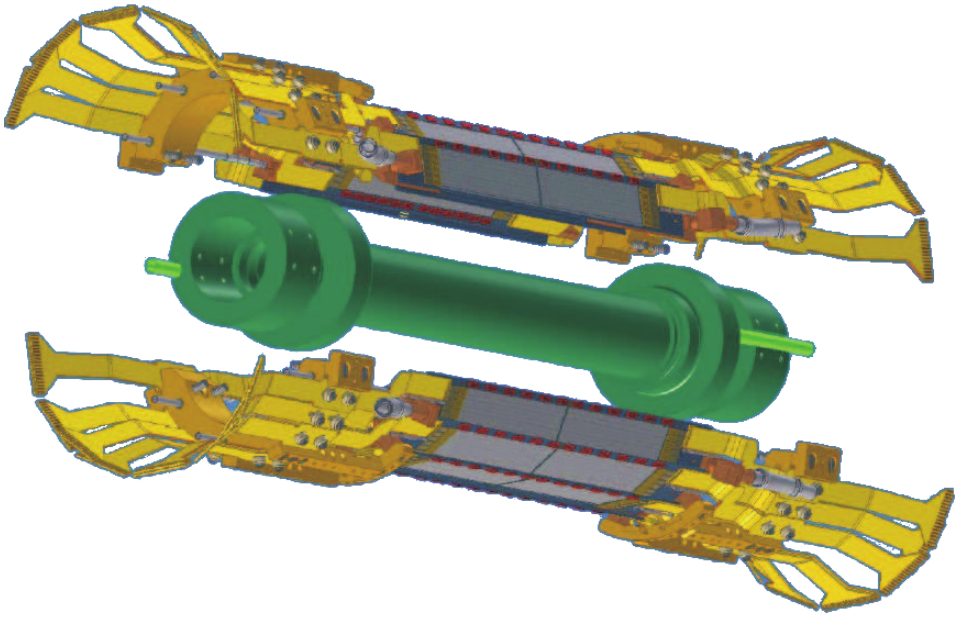

Figure 3.17: Belle II PXD mechanical setup with cooling block and kapton connection. [10]

3.4.3 Read-out and Timing

The detector would suffer from a high occupancy due to the strong beam background radiation. A high readout speed is needed to keep the number of hit pixels per frame low and to make the track reconstruction more robust. This can be accomplished by reading out a frame with 1600 pixel rows within $20\mu s$. The short row read-out time of $12.5ns$ would cause a high noise, as the shaping time in the readout chip has to be very short. The very long (90mm) DEPFET drain lines add noise and have a long settling time, because of their high capacitance. The readout scheme has to be improved without reducing the effective row readout time. A row readout can be slowed down to $100ns$ by using a high degree of parallelism:

- The DEPFET matrix is split in the middle into two halves with 800 rows each. This is also triggered by the module manufacturing, in a first design, where the inner layer modules were not split mechanically, the active area was split electrically. The splitting makes it possible to read out the matrix from both sides, requiring twice the amount of readout electronics, while reducing the row readout time to $25ns$.
- The readout time is reduced even more, by a factor of 4, by reading out 4 rows in parallel. Figure 3.18 shows a half module of the second layer, illustrating the 4-fold row readout. One pair of gate and clear steering signals connects to 4 pixel rows and because the pixel column can't share a common drain line, the number of drains lines has to be increased by a factor of 4, too.

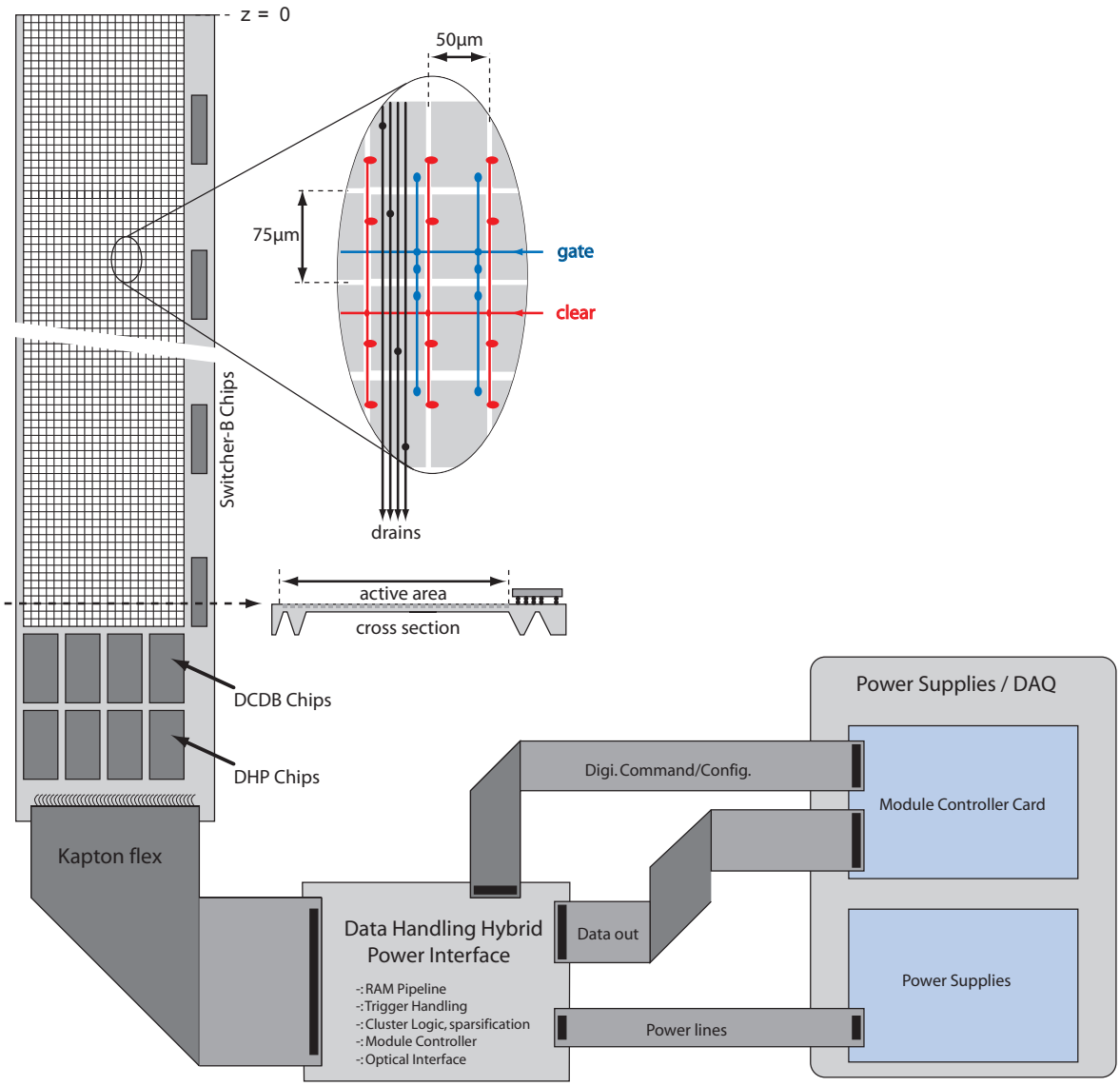

Figure 3.18: Belle II half module drawing with cross section of the thinning, quad row organization, chip location, kapton connection to DHH. [30]

Layer	Number of ladders	power per ladder	power per layer
1	8	18W	144W
2	12	18W	216W
total			360W

Table 3.4: Belle II DEPFET power consumption.

- The gained factor of 8 results in 100ns per row. If the row would be read out in the double-sampling scheme as planned for the ILC detector, the same row would have to be read out twice and cleared in between. Assuming a 20ns clear pulse, the shaping time would be as low as 35ns, which is again too short for low noise sampling. The single sampling scheme has to be used, where 80ns are available for shaping. Single sampling does not remove the offset values from the signal during a row read-out cycle. The offset values have to be stored and corrected at a later point in the readout chain.

The steering chips are located on a balcony on the long side of the matrix. Contrarily to the ILC balcony, only one column of steering chips is used for the Belle detector. The chips for Belle, called Switcher-B (see chapter 5.2), include the clear and gate driver within one chip.

The readout chain contains two chips on the module: The DCDB (see chapter 3.5.2) does a basic offset subtraction and digitizes the drain current values. It's digital output is processed by the DHP (see chapter 3.5.3), which does hit detection to reduce the amount of data. The DHP controls the DCDB and the Switcher-B chips and provides the timing of the readout cycles.

The **D**ata **H**andling **H**ybrid (DHH) receives the Belle II trigger signals for the DEPFET detector and is located outside, but close to the Belle detector. A trigger signal is send to all sub-detectors, if an interesting physics event is detected by the high-level trigger system. The DHH instructs the DHP to send the interesting, pre-readout and internally stored frames with gigabit speed over a kapton flex cable. They are forwarded via an optical fiber to the central data acquisition system and stored for data analysis (figure 3.18).

3.4.4 Module Power Consumption and Cooling

Similar to the ILC design, a Belle II module dissipates most of the power at the end of the module, where the readout chips are located. 4 DCDBs and 4 DHPs per ladder side dissipate 8W. The DEPFET itself produces $\approx 1W$ and the steering chips contributes another $\approx 1W$. Table 3.4 summarizes the power consumption of the vertex detector. [10]

The readout chips are located at the end of the module, which is in direct contact to the support structure. Channels for evaporative CO_2 cooling are integrated within the support structure. They remove heat from the end of the modules directly and cool the chips through the module's silicon and the bump bond connections. Cold dry air is blown through holes in the structure into the gap in between the layers to cool the DEPFETs and the steering chips. As their power dissipation is low, air cooling is sufficient.

3.4.5 Irradiation Damages and Radiation Length

The devices of the pixel vertex detector are located in a harsh radiation environment generated by the high beam current and luminosity. It degrades the detector's performance over time. The radiation damages are much higher than in the ILC and estimated to 1-2 Mrad of ionizing radiation and $10^{13} n/cm^2$ 1MeV neutron equivalents per year. Exact numbers on radiation are not available as accelerator parameters are still subject to change.

Single DEPFET transistors have been irradiated up to 10Mrad, to include a safety margin, and show a threshold shift of up to $\approx 20V$ after 28 days annealing[31]. This high voltage shift has to be supported by the steering chip and power supplies, otherwise the detector would render useless.

A second option for reducing the negative effects of irradiation is currently evaluated by the DEPFET developers. A thinner gate oxide on the transistors reduces the threshold shift after irradiation dramatically to only $3V$. The thinner oxide increases the gate capacitance, which reduces the internal amplification g_q. This can be compensated by a reduction of the gate length. The thin oxide option will be used for the final production of the DEPFET matrixes.

As the experiment is very asymmetric, an acceptance angle of 17 degrees forward and 150 degrees backward, the irradiation of the DEPFET matrix is expected to be non-uniform. This causes different threshold voltage shifts lengthwise, which could make it impossible to tune the gate voltages to an optimum for all DEPFET transistors at once. The gate control voltages will be divided into three segments to provide the optimum voltage for every region. [10]

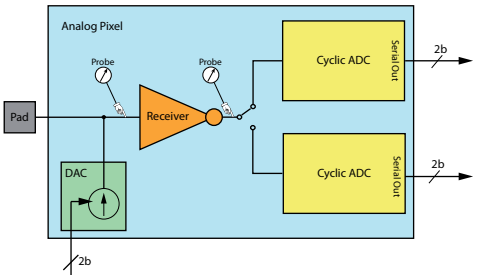

Figure 3.19: Block diagram of a DCDB input cell. [33]

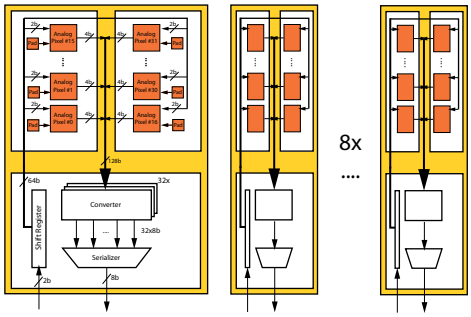

Figure 3.20: Block diagram of the 8 DCDB slices of 32 inputs each. [33]

3.5 Read-out Chips for DEPFET modules

The readout chip is a custom build ASIC[3] adopted to particular detectors requirements. It amplifies and digitizes the detector's signals. The current readout chip called **D***EPFET* **C***urrent* **D***igitizer* (DCD) is the successor of the **Cu***rrent* **R***ead* **O***ut* (Curo) shown in figure 3.1. A successor was needed as the Curo wasn't designed for the high capacitance of large matrixes' drain lines, showed a high noise and had no ADC yet.

3.5.1 Curo

The Curo was designed at the SiLab semiconductor group at Bonn University and implements the double sampling readout scheme and a hit detection. The double sampling subtraction is realized in the current domain by current memory cells storing the DEPFET drain current before and after clearing. The resulting signal current is stored in an analog FIFO and can be shifted out to be digitized by an external ADC. A threshold value defines the signal level of pixel considered to be hit by a particle. Pixel addresses of hit pixels can be read out digitally during the long bunch pause. Detailed information can be found in [32].

The chip's digital part is designed for running with $100MHz$ and allows a double sampling readout with a row frequency of $25MHz$. It is manufactured in a $0.25\mu m$ process and is radiation tolerant for the expected low dose at ILC. The Curo's measured noise value of $100nA$ corresponds to $250e^-$ ENC for a DEPFET amplification of $400pA/e$.

3.5.2 DCDB

The DCDB is an advancement of the DCD2 read-out chip and is designed for the Belle II experiment. It is a full size, close to final chip with a $5mmx3.2mm$ large die and 256

[3] **A**pplication-**S**pecific **I**ntegrated **C**ircuit

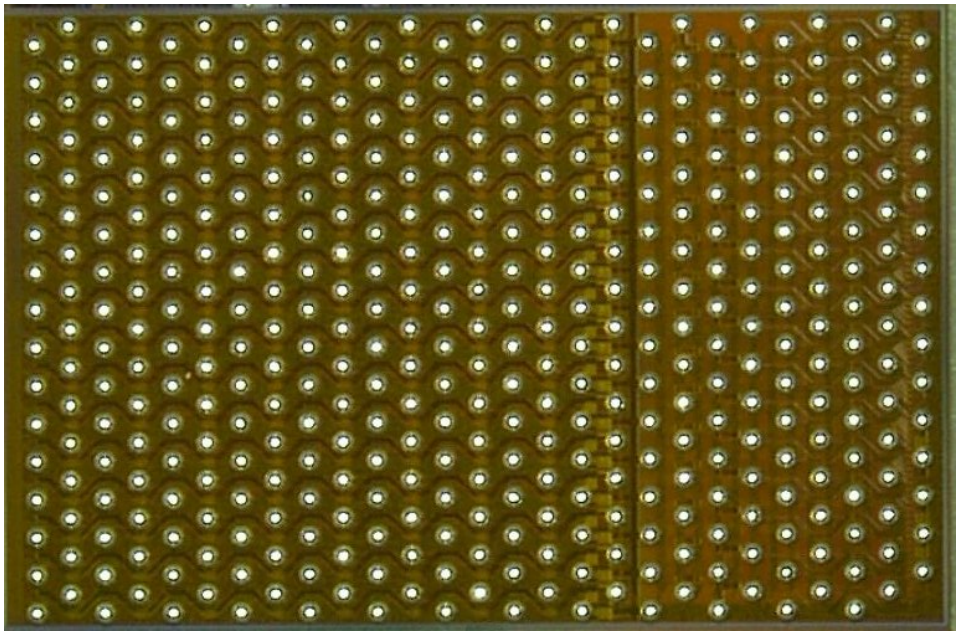

Figure 3.21: Photograph of the 5mm x 3.2mm large DCDB readout chip with 256 inputs and eight 8 bit outputs.

inputs. Commercial solder bumping became available for the 180nm UMC multi project submission and has been chosen as interconnection technology. The regulated cascode has been replaced by a trans-impedance amplifier with a programmable gain. It allows to adjust the ADC range to the signal range and keeps the input potential constant. The DEPFET detector signals, in the range of $3\mu A$, have to be read out with a signal sampling time of $< 100ns$ ($> 10MHz$). Two ADCs per input are used to achieve this speed. They digitize sampled signals alternatingly (figure 3.19) and run at low speed to achieve a low noise value. A current source, controlled by a 2 bit DAC, is included in every input cell. It roughly compensates pedestal fluctuations of the DEPFET matrix and adopts the drain current to the dynamic range of the ADCs.

The digitized signals of 32 input cells, with 2 ADCs each, are serialized to a 8 bit parallel link. The link runs at a speed of up to $400MHz$, which is defined by the ADC conversion time. Eight slices of 32 inputs are included in one chip (figure 3.20). In total, one chip running at 100ns sampling time generates a data-rate of $2.56GB/s$. The DACs for pedestal correction have to be set externally for every conversion cycle. Including on-chip memory was not possible due to space limitations.

The digital part of the DCDB has been tested and operates at the target speed of $320MHz$ correctly, with a noise of $90nA$ and a ADC resolution of 6 bits. For more detailed information it is referred to [34],[33] and [35].

The analog part, from the input up to the ADCs, is a full custom design, while the processing of the ADC output and multiplexing in the digital domain is an automatically

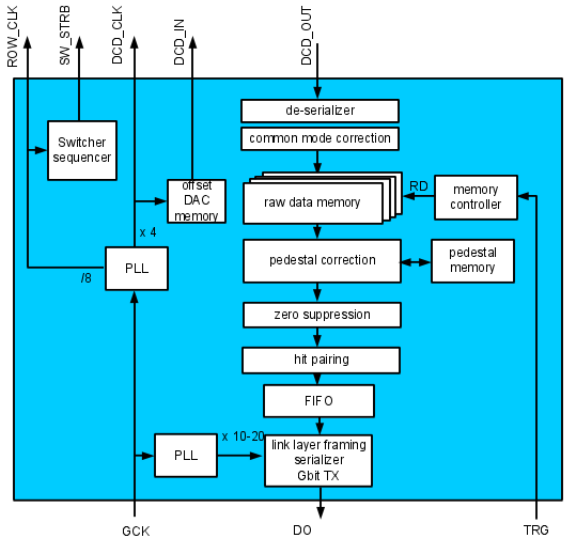

Figure 3.22: Block diagram of the DHP data processing chip. [36]

placed and routed standard cell design. A JTAG interface is integrated to configure and test the chip. It allows access to the control registers and the boundary scan chain. A $180nm$ $1.8V$ technology with 6 metal layers is used for the DCDB, which also provides an additional 7th metal layer with solder bumps (see figures 3.21). The 7th metal layer is used as a redistribution layer, originally meant to add solder bumps to a wire-bond only design and route the signals from the wire bond pads to the bump bond pads. This layer was used to connect the bump pads to the input cells directly. Following the manufacturers design rules, a pitch of $\approx 200\mu m$ could be achieved using lead-free SnAgCu solder material and screen printing technique. The bump pattern was designed and matched to the wire bond adapter layout as part of this thesis (see chapter 6.6).

3.5.3 DHP

The DCDB's raw ADC values cause a data rate of $2.56GB/s$ per chip, which sums up to $10.24GB/s$ for a module with 4 chips. This exceeds the transmission capability of the DEPFET module's connection to the data storage and physics processing devices. Therefore, a data reduction needs to be introduced: The **D***ata* **H***andling* **P***rocessor* (DHP) is being designed by the SiLab group at Bonn University and will reduce the data-rate to a single $1Gbit/s$ link per DCDB. Every DCDB will be connected to a DHP. The DHP will realize the data reduction by using zero suppression and hit pairing. It is a synthesized chip build in a $90nm$ IBM CMOS technology with solder bump provided by IBM in the C4 process. Figure 3.22 shows the block diagram of the chip. The DCDB's data is de-serialized, corrected for matrix common mode noise and continuously stored in on-chip memory. A trigger signal starts the frame processing. The pixel pedestals are

corrected for using on-chip stored values and a zero suppression reduces the amount of data by discarding all pixels with signals below a threshold value. Then, a hit pairing algorithm is used to find neighboring pixels which show a signal. The neighboring pixels are needed to apply the center-of-gravity algorithm. Only one pixel address and an orientation bit is transmitted for a hit pair. A serial current mode logic $1Gbit/s$ link, implementing the the Xilinx Aurora 8B/10B protocol, transfers the data to a Xilinx FPGA. As the physical parameter of the particle accelerator are not fixed yet, the chips properties, e.g. the data rate, might change. [36]

The DHP is the controller for the DCDB and Switcher-B steering signals. The Timing of the DEPFET row gate and clear signals and the DCDB control signals have to be exactly controlled, to know the position of the processed data within the DEPFET pixel matrix. It is also a controller for the JTAG slow control signals of Switcher-B and DCDB.

4 Read-out Chip Design & Characterization

4.1 DCD for ILC

A successor for the Curo had to be developed, as the Curo can't handle the high capacitance of large matrixes. The **D***EPFET* **C***urrent* **D***igitizer* (DCD) follows a different approach. It integrates multiple analog-to-digital conversion circuits and outputs the digitized current values. The prototype chip developed at the Chair of Circuit Design of Heidelberg University has 72 input channels arranged in a 6×12 matrix. Each channel is using 2 current-mode cyclic ADCs with 8 bit resolution. The ADCs are operated in parallel to increase the sampling rate. Each input channel is $180\mu m \times 110\mu m$ small and contains a bump pad of $60\mu m$ diameter, which uses most of the area. Twelve differential digital outputs transmit the serialized ADC data with $600Mbit/s$ LVDS transmitters. The chip is a full-custom design in a $180nm$ process and has an overall size of $1525\mu m \times 3240\mu m$ (see figure 4.1).

A current only signal path from the input to the ADCs allows a direct processing of the DEPFET's drain current. Figure 4.2 shows a part of the signal path of a channel. The current input bond pad is located on the left. A current sink (VNMainOffset) subtracts a coarse amount of the DEPFET's pedestal current in the range of $50 - 100\mu A$. The current sinks share the same setting and thus cannot be adjusted per channel. They are

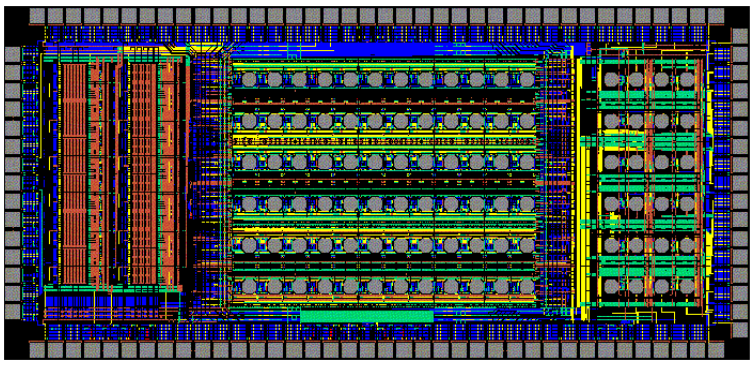

Figure 4.1: Photograph of the 1.5mm x 3.2mm large DCD2 readout test chip with bump bond pads and additional wire bond pads for testing.

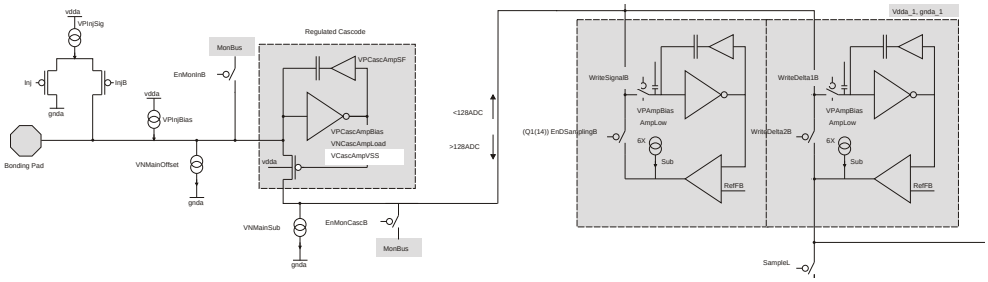

Figure 4.2: Block diagram of input, regulated cascode and current memory cells for double sampling of DCD2. [37]

used to adjust the input to the dynamic range of the regulated cascode. The cascode receives the DEPFET current and keeps the input node at constant potential. This allows a fast settling of the current on the high capacitance of the drain lines after switching the DEPFET pixel matrix to another row. An injection circuit is used to simulate a DEPFET's signal during chip testing.

The next parts in the processing chain are the two current memory cells shown on the right of figure 4.2, which are used for the double sampling readout scheme. The left memory cell stores the pedestal+signal current, if double sampling mode is enabled. The right memory cell is enabled after clearing the DEPFET's signal charge and stores the difference of the baseline current flowing from the DEPFET and the current stored in the left memory cell.

The current is then transferred to the 8-bit cyclic ADC. Two ADCs are digitizing the sampled currents alternatingly to speed up the digitization while running the ADCs themselves at a lower speed for a better signal-to-noise ratio. The bit streams of all ADCs of one column are multiplexed to one of the six high speed differential outputs.

The first test chip DCD1 suffered from a too small supply metal line, which caused a high voltage drop across the input cell matrix. This rendered the chip unusable and made a production of the DCD2 necessary. The following measurements were done with the DCD2 chip. More detailed information on the chip can be found in [34].

4.1.1 Measurements

Test setups for the DCD1 and DCD2 have been developed as part of this thesis. An add-on PCB for the Uxibo FPGA board has been designed (see figure 4.3). The chip is wire bonded to the PCB. Several bias voltages and currents are generated on-board and the LVDS outputs are converted to single ended CMOS levels for compatibility with the FPGA board. A speed limit of $48MHz$ is implied by the FPGA board. The debug modes of the DCD allow a bypassing of the internal clock dividers and the output multiplexers. One ADC of a column can thus be operated with $48MHz$. This is just half

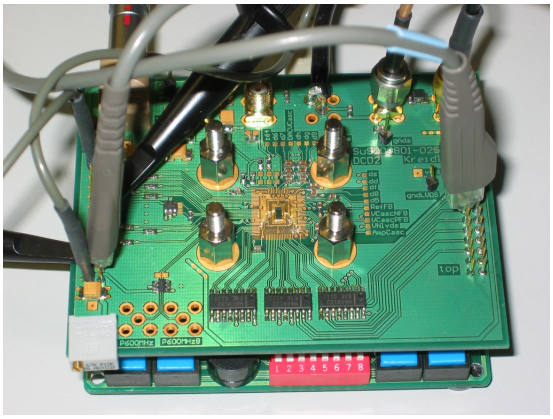

Figure 4.3: Photograph of the DCD Test PCB.

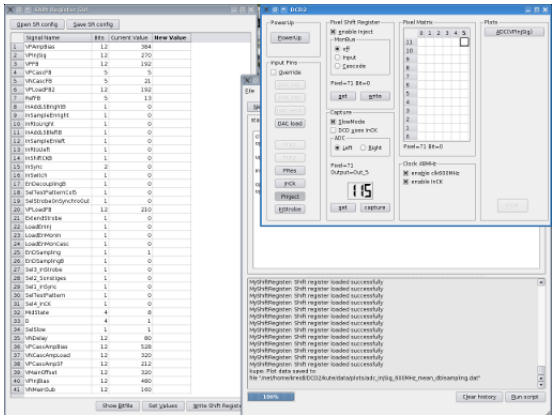

Figure 4.4: Screenshot of the DCD Test Software.

of the anticipated speed, but sufficient for testing the functionality of the new readout approach. Measurements with a later test setup running at high speed can be found in [38].

Figure 4.5 shows the range of the input current which can be sunk by the regulated cascode, while keeping the input potential constant. A current of at least $16\mu A$ can be handled, while the voltage changes only by $4mV$. Most of the incoming DEPFET baseline current has to be subtracted by the current sink in front of the cascode, in order not to exceed this $16\mu A$ range.

The current memory cell measurement in figure 4.6 shows the current storage range. It shows a good symmetry and can source and sink currents of up to $8\mu A$. An additional current sink (VNMainSub, figure 4.2) is used to shift the input current range from the cascode's $0...16\mu A$ to the memory cell's range of $-8...8\mu A$.

The ADC response has been measured by sourcing a current with the build-in DAC controlled test current source (VPInjSig) at the input node of a channel. Its current has been measured first. Figure 4.7 shows the ADC's response as a function of the measured test source's current. It is linear and uses the ADC's full 8 bit range. Many ADC samples have been taken for every current source DAC setting. The deviation from their mean value is shown in figure 4.8. A current noise of $46nA$ has been calculated.

4.1.2 Irradiation of DCD2

The chip has been irradiated with X-rays ($66kV$ $33mA$) up to a dose of $3.5Mrad(SiO_2)$[1] to simulate radiation damages during operation in the particle accelerator. It was operated and biased during the irradiation to ensure realistic results. The irradiation also

[1] radiation absorbed dose; $1rad = 0.01Gy = 0.01\frac{J}{kg}$

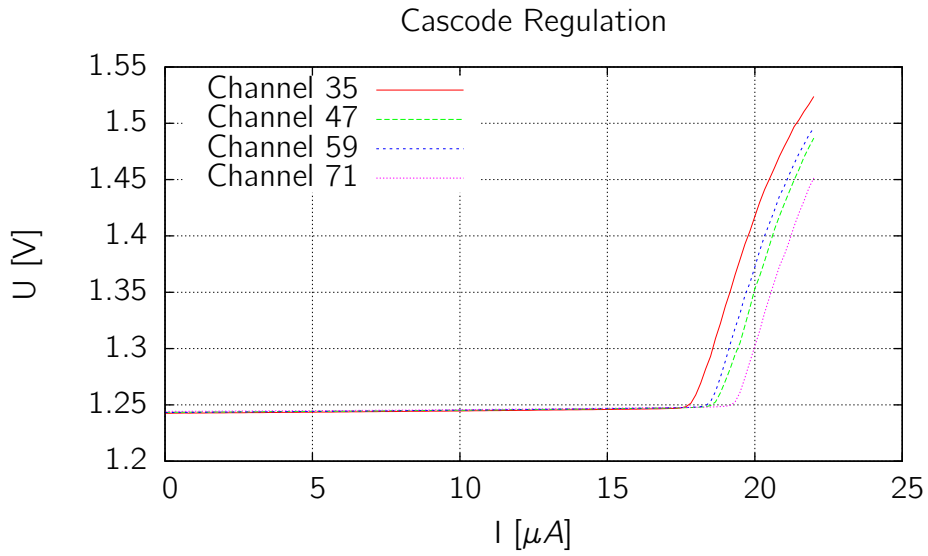

Figure 4.5: Measured voltage at the regulated cascode input as a function of the measured injection current. The input voltage is constant in a current range of up to $17\mu A$. 4 input channels are shown.

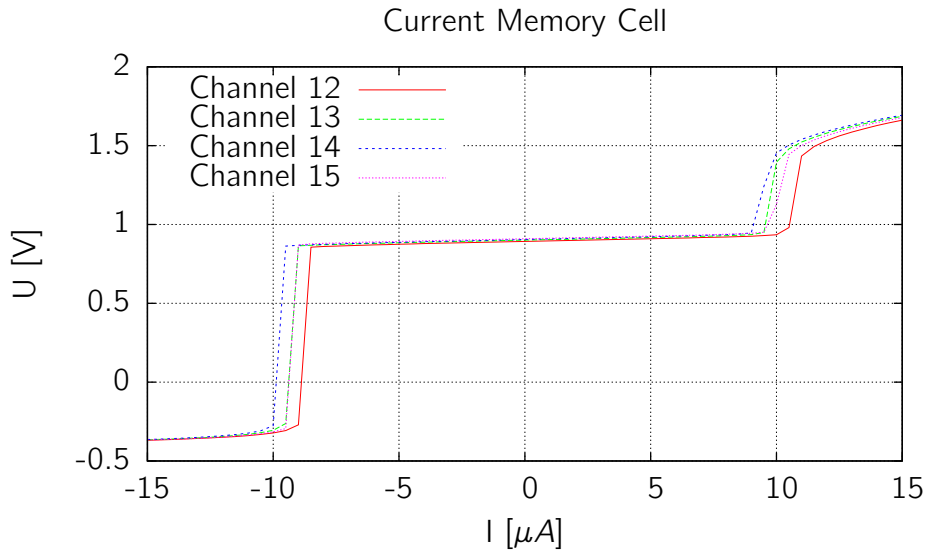

Figure 4.6: Measured voltage at the DCD2 Current Memory Cell input as a function of the measured injection current. The cell is able to sink and source currents in the range of $-8...8\mu A$.

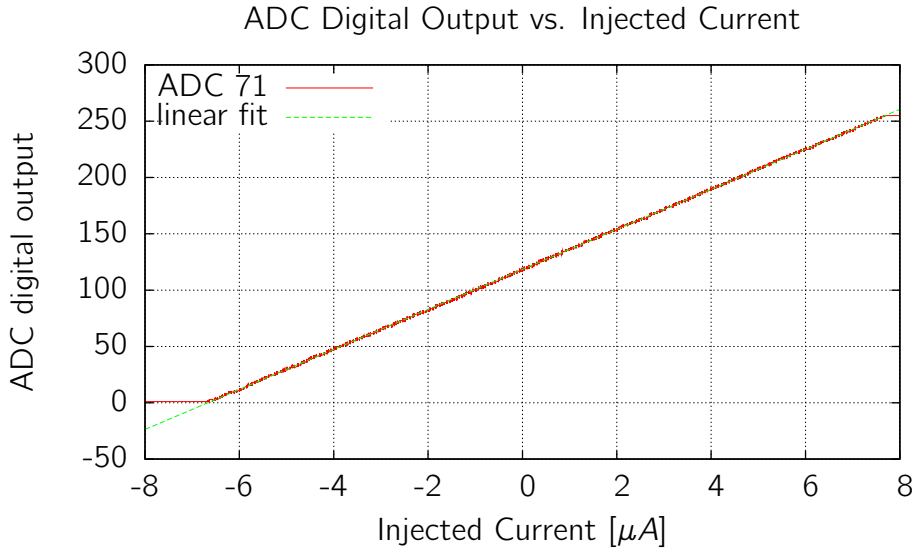

Figure 4.7: DCD2 ADC digital output as a function of the injected current.

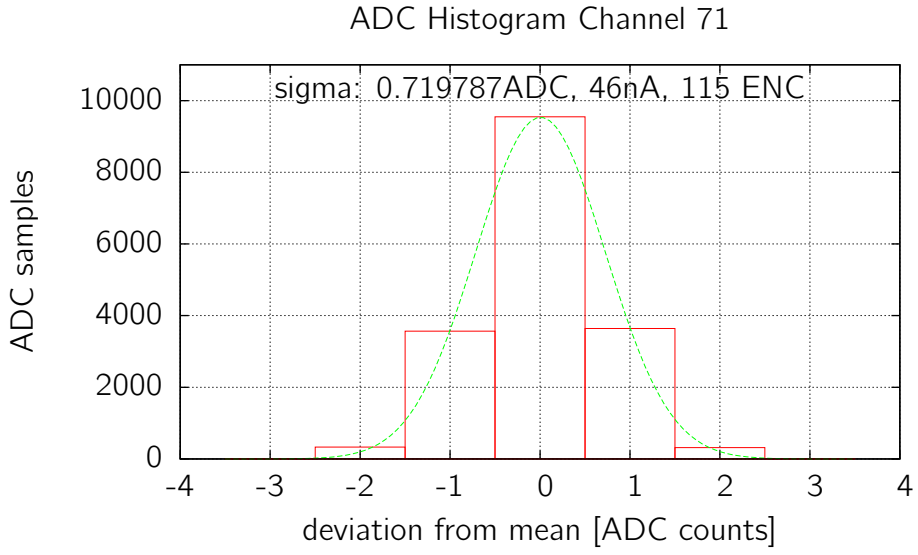

Figure 4.8: DCD2 ADC histogram showing deviation from mean of several ADC samples running at 48MHz. Sigma of $0.7ADC \leftrightarrow 46nA \leftrightarrow 115ENC$ with $g_q = 400pA/e^-$

Dose	Noise [ADU]	Noise [nA]	Noise [ENC]
0 krad	0.61	39	98
568 krad	0.55	35	87
3.5 Mrad	0.64	41	102
6d anneal	0.61	39	97

Table 4.1: ADC Noise for different doses.

influences the built-in DAC controlled current injection circuits. Equal DAC settings will generate different currents with an increasing dose. The currents have to be measured before an ADC characterization to compensate for the radiation induced current changes.

Figure 4.9 shows the ADC response as a function of the injected current for doses of $568krad$ and $3.5Mrad$, as well as before irradiation and after 6 days of annealing at room temperature. Peaks occurring at $568krad$ and $3.5Mrad$ are believed to be single event upsets caused by the high intensity X-ray beam, as measurements were taken with an activated beam. The ADC gain increases with the deposited dose and recovers completely to the pre-irradiated state after a 6 days annealing period.

62 ADC values have been recorded for each injection DAC setting. The deviation from their mean values is displayed in figure 4.10 at different doses. Table 4.1 lists the corresponding noise values. The low noise value for the $568krad$ measurement is caused by a large decrease of the injected current, which is outside the ADCs range. It recovers with increasing dose. The noise increases with the dose and recovers to the pre-irradiated state after the annealing period.

The measurements show that the new readout chip is working and is radiation tolerant up to at least $3.5Mrad$.

4.2 DCD-RO

The DCD-RO is a level converter, driver and multiplexer chip. It has been designed and tested during this thesis. It is needed to test the DCDB standalone, without the DHP. The DCDB uses low voltage swing, single ended outputs to send the data to the closely located DHP, with a signal path of only 1-2mm length. It is not possible to connect the DCDB directly to a PCB and a FPGA, because of the high capacitive load of traces and FPGA inputs. The DCD-RO was introduced as an interface between low swing DCDB and FPGA compatible LVDS signals. A multiplexer had to be included into the chip, because the number of chip connections doubled with the use of differential pairs and the chip size was confined to limit costs. It allows to read out half of the DCDB channels at once. To be able to read out DEPFET matrixes in test systems without switching the multiplexer, the four middle or the two left and right slices can be selected. The left

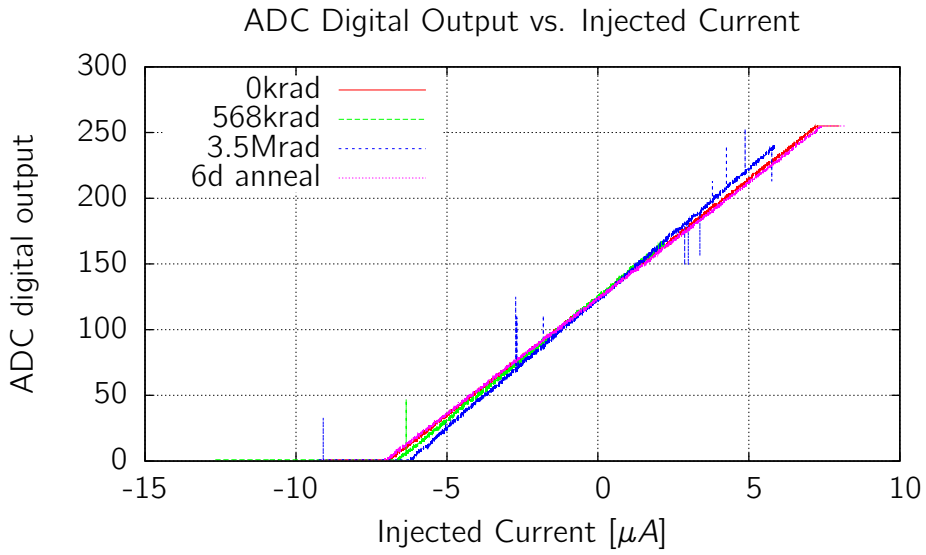

Figure 4.9: DCD2 ADC digital output at different doses as a function of the injected current.

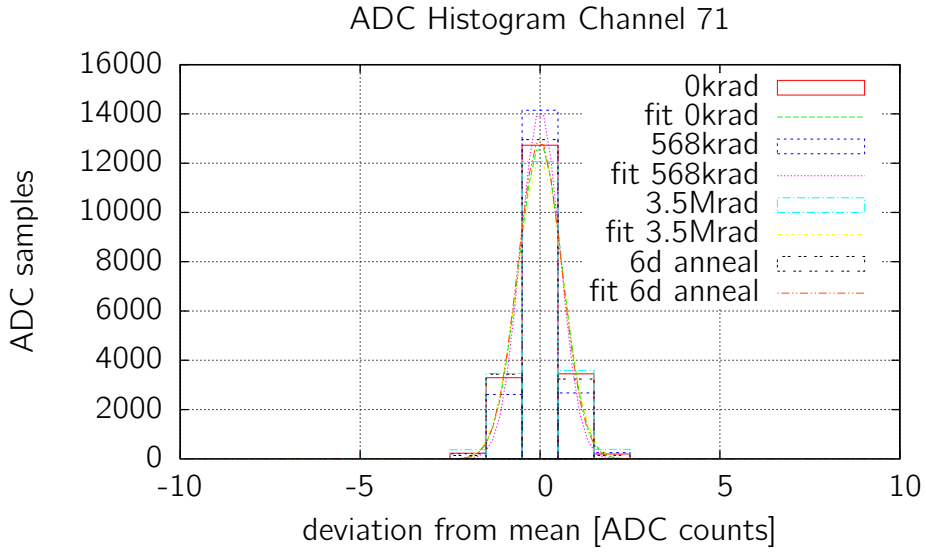

Figure 4.10: DCD2 histogram after irradiation at different doses.

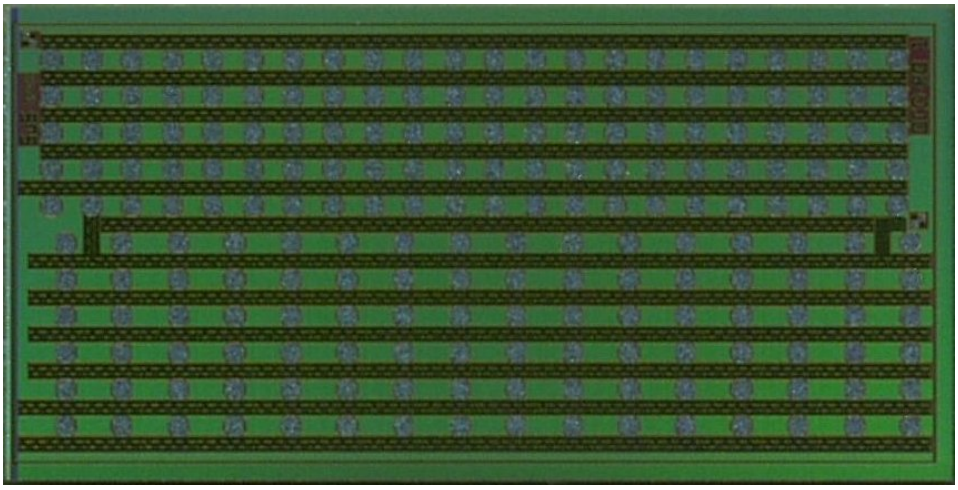

Figure 4.11: Photograph of DCD-RO Chip with a size of $3240\mu m \times 1525\mu m$.

and right slices are not available on the wire bond adapters, because the routing of the DCDB JTAG signals block the access to the data pads on the single metal layer layout. Only the middle slice can be wired on these wire bond adapters (see figure 6.27 on page 96).

Figure 4.11 shows a photograph of the $3240\mu m \times 1525\mu m$ chip designed in a 180nm process, which fits the width of the DCDB. It uses bump bonding to be connected to a wire bond adapter and is placed closely to the DCDB. Gold stud bumps have to be used, because they allow a smaller pad pitch needed for the many LVDS connections (see chapter 6). The pads connecting to the DCDB are located on the lower half, while the LVDS pairs are placed on the upper half. Different pad pitches are used for LVDS and DCDB pads to match space constraints and allow for easy routing, respectively.

The block diagram in figure 4.12 shows the connection of the data outputs of the DCDB slices to the multiplexer, the distribution of offset correction DAC signals and the control signals. Differential receivers are used for the low swing single ended signals, with a reference voltage supplied by the DCDB to securely define the switching point. After passing the multiplexer, the CMOS signals are converted to LVDS. Offset correction values transferred from the FPGA to the DCDB are converted to CMOS and distributed. Both halves of the DCDB get the same offset values. No registers or multiplexers are used.

Reducing the power consumption was not a design goal, as the DCD-RO is only needed for DCDB testing and characterization and won't be used in the final detector modules.

A test setup has been designed to operate the chip stand alone. The chip has been wire bonded to the PCB directly. Not all in- and outputs could be connected, but critical steering signals and some data signals to test the multiplexer were attached. $400MHz$ test signals have been generated by a pulser with CMOS and LVDS output

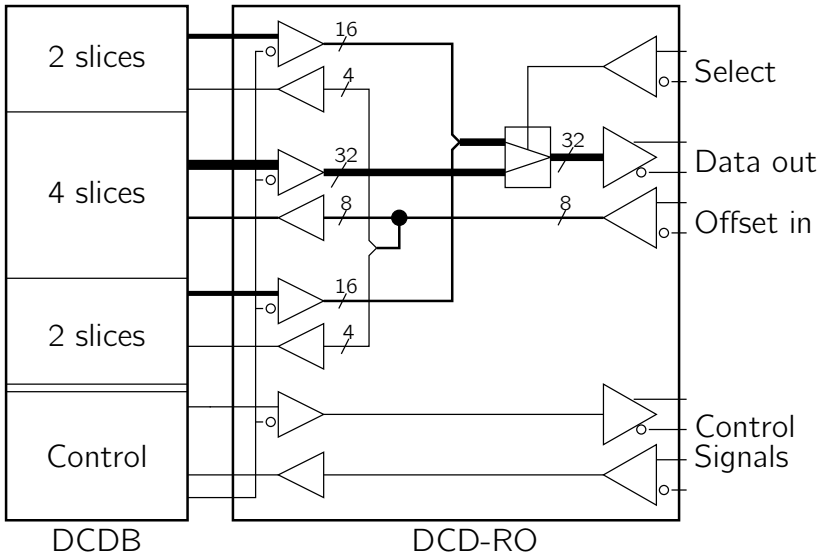

Figure 4.12: DCD-RO block diagram.

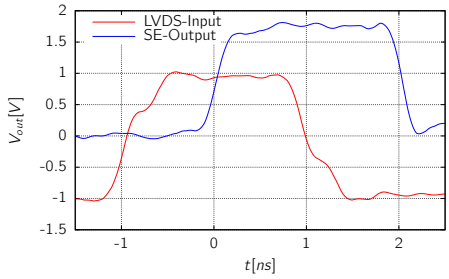

Figure 4.13: Measured DCD-RO propagation delay of $1ns$ from LVDS-input to single ended output.

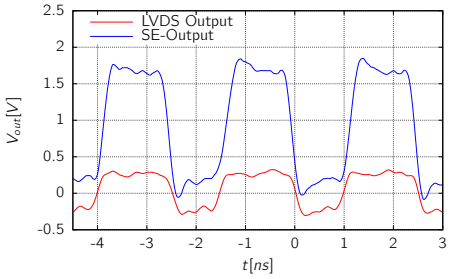

Figure 4.14: Measured DCD-RO LVDS- and single ended outputs running at 400MHz.

and were connected to the appropriate chip inputs. The outputs were monitored with an oscilloscope. The DCD-RO is able to convert $400MHz$ signals on all connected paths. Figure 4.14 displays two $400MHz$ clock signals at the the chip's LVDS and single ended outputs, measured with a differential and single ended probe respectively. The propagation delay of $\approx 1ns$ is shown in figure 4.13. The multiplexer is switching correctly, although its input was accidently inverted at the design phase.

The DCD-RO is an important ingredient for testing the DCDB alone and for matrix read-out. When bonded to wire bond adapters together with the DCDB, it allows a high speed communication up to the DCDB's limit of $320MHz$ [35].

5 The Switcher Steering Chips

A specially designed ASIC is needed to enable the read-out of the signal and to clear the stored charge of the DEPFET's internal gate. The amount of steering lines, as well as timing, space, material and radiation constraints don't allow the use of commercial components to fulfill the steering tasks.

The 'Switcher' steering chips have been developed to fit to the needs of the DEPFET matrixes. Several versions of this chip have been developed at the Chair of Circuit Design. The basic principle of all versions is the row-wise addressing of the chip's output channels and the controlling of the gate and clear signals, by either dedicated strobe inputs or by build-in generators. As the DEPFET's control voltages are high compared to the operating voltages of VLSI[1] semiconductors, a high voltage technology or an advanced circuit design is mandatory. Several steering chips are needed on large DEPFET modules to control all matrix rows, so that a chip synchronization has to be implemented.

The following list presents the different versions of the chip with their major differences:

- The first version of the *Switcher* has been developed in a $0.8\mu m$ high voltage technology. It includes 64 output channels, each with 2 independent outputs for gate and clear signals. An integrated memory allows to program output switching sequences. The channels are selected sequentially and a daisy chaining of chips is implemented by external signals indicating to the neighboring chip to start switching. [39]
- The *Switcher II* is a redesign of the first version in a smaller $0.35\mu m$ high voltage technology. The chip has the same functionalities as the *Switcher I*.
- An enhancement has been introduced with the *Switcher IIb*: Small switches can connect each output to a monitoring bus to simplify testing of the chip functionality prior to connecting it to DEPFET matrixes and to provide monitoring possibilities during operation. The test setup for characterization of *Switcher IIb* and mass tests has been developed in the authors diploma thesis [40].
- A weak radiation tolerance, slow speed and the flip-chip incompatible layout of the *Switcher IIb* made the development of the *Switcher3* for the ILC detector necessary. It uses a completely different approach for the high voltage outputs by using faster standard transistors with an advanced circuit design instead of simpler high voltage

[1] **V**ery **L**arge **S**cale **I**ntegration

transistors. A programmable sequencer can address the output channels directly in arbitrary sequences, a feature that was desirable at that time. Contrarily to previous Switchers, the Switcher3 has only one output per channel, but 128 channels per chip. A flip-chip compatible layout is used with additional wire bond pads in the design phase.

- The requirements changed during the matrix development for the Belle II detector and triggered a new chip design. It uses special radiation tolerant HV-transistors to switch the high voltage and a low power level shifter design.

5.1 Switcher3 for ILC

The high occupancy in the pixel detector for the ILC project made a faster Switcher chip necessary. The matrix has to be read out more often in order to reconstruct particle tracks precisely. A high radiation background of a few hundred krad per year contributes to the detector occupancy and also to the radiation damages in the semiconductor devices. Especially the Switcher IIb is susceptible to radiation induced damages. The $0.35\mu m$ high voltage technology with its thick gate oxides and no radiation tolerant design caused the first failures at a dose of 18krad, when the build-in RAM failed. The chip showed increasing power consumption and output transistor degradation within only 50krad [40].

A new approach has been developed with the Switcher3. It includes more intelligence into the Switcher, enabling it to address matrix rows by a programmable sequencer. A radiation tolerant design is used throughout the chip. High voltage transistors with thick gate oxides have been avoided. Thus, the operating range of the output stage is limited, but is still compatible with the ILC matrix requirements.

A test setup has been developed as part of this thesis, the chip was carefully characterized and its radiation tolerance has been evaluated.

5.1.1 Architecture and Design

Figure 5.1 shows the photograph of the $5780\mu m \times 2255\mu m$ large chip. It is designed to be connected to the matrix using flip-chip bonding. The octagonal bump pads are located in the center of the die. Additional wire bond pads have been added to be able to test the chip with existing, non flip-chip matrixes. The silicon area covered by the rectangular wire bond pads does not contain any circuits, allowing the pads to be easily removed for the final chip production. The chip size is reduced to $5780\mu m \times 1400\mu m$ without these pads.

The control signals are located at the bottom of figure 5.1 and the 128 outputs are arranged in a 4×32 bump pad array. Contrarily to the Switcher II, an output channel

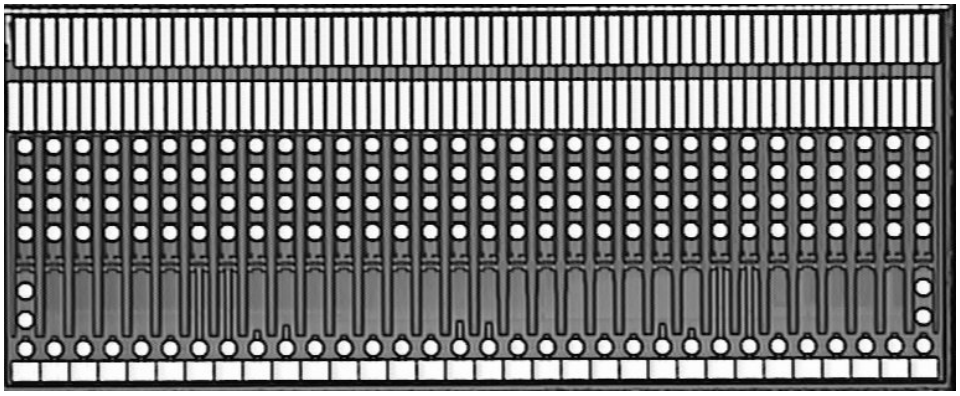

Figure 5.1: Photograph of the Switcher3 die.

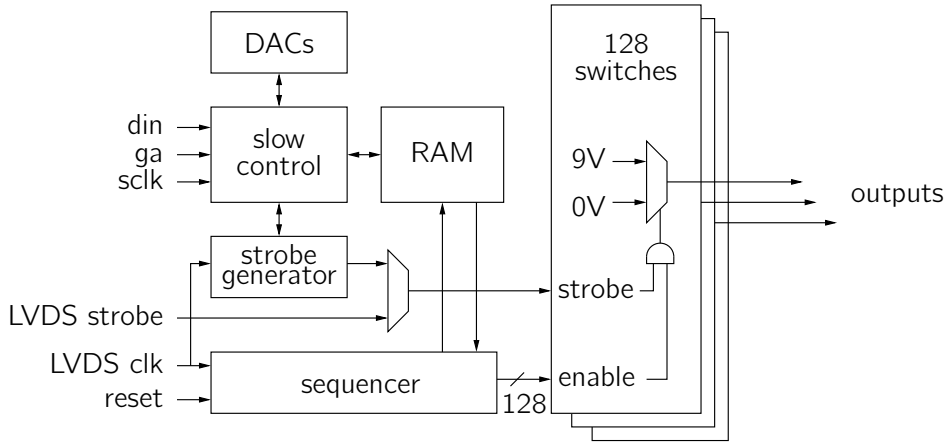

Figure 5.2: Switcher3 top-level block diagram.

contains only one output switch. Two chips are needed to provide the gate and clear steering signals, as shown in figure 3.10 on page 29. The single output design was chosen, because it simplifies the chip design with respect to the voltage levels within a chip and the amount of bump pads.

As a consequence, a tricky circuit had to be invented which can switch up to 10V with transistors with a maximum operation voltage of 3.3V (see section 5.1.3). A 10V switching voltage had been considered sufficient for the DEPFETs intended for the ILC.

Figure 5.2 shows the top-level block diagram. A simple slow control interface with a serial protocol is used to configure the chip. The sequencer program can be written into the RAM, the DACs and the delay of the strobe generator can be set. The 128 output drivers are enabled by a select signal generated by the sequencer. The timing of the edge can be tuned by either an external strobe signal or by using the build-in strobe generator. This generator is a programmable delay element and is triggered by the sequencer's clock signal.

An enclosed transistor layout has been used together with guard rings to prevent a malfunction in the radiation environment of the ILC experiment. A smaller amount of charge is trapped in thin gate oxides of standard transistors and thus the threshold shifts are smaller. Single event upsets (SEU) are storage cell value changes, that are caused by large amount of charge generated punctually by ionizing radiation. This can alter the chip's configuration, which can lead to unexpected behavior or can destroy the output driver circuits. Additional Hamming bits to correct such single bit errors in the RAM were foreseen, but not implemented in this chip revision [41].

5.1.2 Sequencer

The sequencer is programmable with a small command set of conditional and unconditional jump command, register load and branch commands. This allows flexible access to matrix rows, e.g. to selectively read out matrix regions with a higher occupancy more often than others or to skip defective matrix rows. Looping is done by initially loading a 8-bit value into one of eight registers and calling the BNZDEC command. This command jumps to the given address, if the register value is not equal zero and decrements the register's content by one. Otherwise, it continues with the next command. It is possible to implement up to eight loops with the load and branch commands. A conditional jump command jumps to the given address if an external chip input signal is set, acting as an interrupt to change matrix readout cycles, e.g. to a triggered region of interest (ROI) read out. The RAM can store a program length of 64 commands.

```
0 jump 1 onabs 13
  jump 2 onabs 17
2 jump 3 offabs 17
  jump 4 onabs 13
4 jump 5 onabs 13
  jump 6 onabs 17
6 jump 0 offabs 17
```

Listing 5.1: Example sequence using jump commands and absolute channel addressing. The output is shown in figure 5.3.

Every command controlling the program flow includes also a channel command. This selects or deselects the active output channel. An absolute or relative addressing can be used. Listing 5.1 shows a loop of 7 commands with an absolute addressing of channels 13 and 17. The sequence runs at the maximum speed of 150MHz and the resulting output is shown in figure 5.3. Listing 5.2 shows a loop example where all 128 channels are enabled consecutively using relative channel addressing.

All commands have been successfully tested.

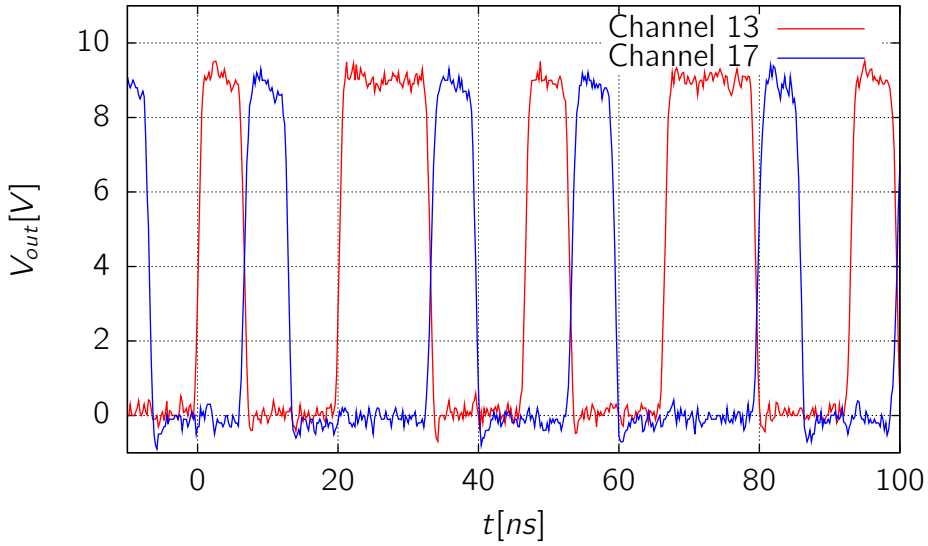

Figure 5.3: Measured sequence from listing 5.1 with $0pF$ load and $150MHz$ clock frequency. The sequence starts at $t = 0$ and repeats every 7 clock cycles.

```
0 load a1 125 onabs 0
  bnzdec a1 1 on 1
2 jump 0 on 1
```

Listing 5.2: Example sequence looping through all output channels and using relative channel addressing.

5.1.3 Output Stage

The output driver's high voltage transistors used in Switcher II have been replaced by standard transistors with a thin gate oxide. These are less susceptible to radiation induced threshold voltage shifts.

An output voltage swing of up to $10V$ is required by the DEPFET matrix. Three transistors are connected in series, in order to not exceed the maximum allowed gate-source and drain-source voltages at each transistor. Therefore, each transistor gate is powered with a separate voltage. Figure 5.4 shows the transistor gate voltages for switching the channel output on and off. The middle transistor gates are kept at a constant potential, while the others must be switched. Level shifting circuits are needed to provide the appropriate gate voltages to the transistors, because the digital enable signal has only a $3.3V$ level. Conventional current based approaches cause a static power consumption, which had to be avoided to save power. A capacitive coupling has been used. Figure 5.5 shows the coupling capacitor, which is used to flip a node of a

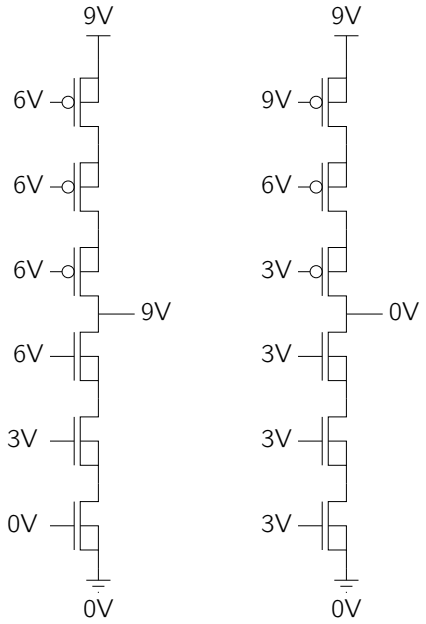

Figure 5.4: Switcher3 output stage gate voltage configuration for on and off state, for $0V$ and $9V$ output voltages.

SRAM cell. A reset switch is used to define the initial state of all SRAM cells, prior powering-up the output supply voltages. Without resetting, all stacked transistors could be switched on simultaneously, causing a high cross current flow which can destroy the output transistors.

The output stage has to provide fast signal edges to meet the ILC readout speed goal of $50ns$ per row. Four signal transitions are used in the sample-clear-sample readout mode: the gate-on edge, the two edges of the clear pulse and the gate-off edge. For sufficient signal sampling time before and after the clear pulse, the transition time of the edges should be less than $10ns$. A capacitive load on the gate or clear matrix lines of $20pF$ is expected and designed for.

Figures 5.7 and 5.6 show the measured falling and rising edges of an Switcher3 output channel with 9V swing for different load capacitors. The measurements show that the Switcher is capable of driving a $22pF$ load within $7ns$.

The power consumption on the digital supply is shown in figure 5.8 as a function of the clock frequency. It shows the expected linear behavior with a static contribution caused by the LVDS receivers of the differential clock and strobe input signals. It also depends on the LVDS bias DAC setting.

Figure 5.9 shows the power consumption on the 9V supply as a function of clock frequency for different load capacitors. It was measured by constantly cycling through multiple channels, which were connected to the load capacitors. The measurements show a linear behavior with no static power consumption. The non-linearity with the

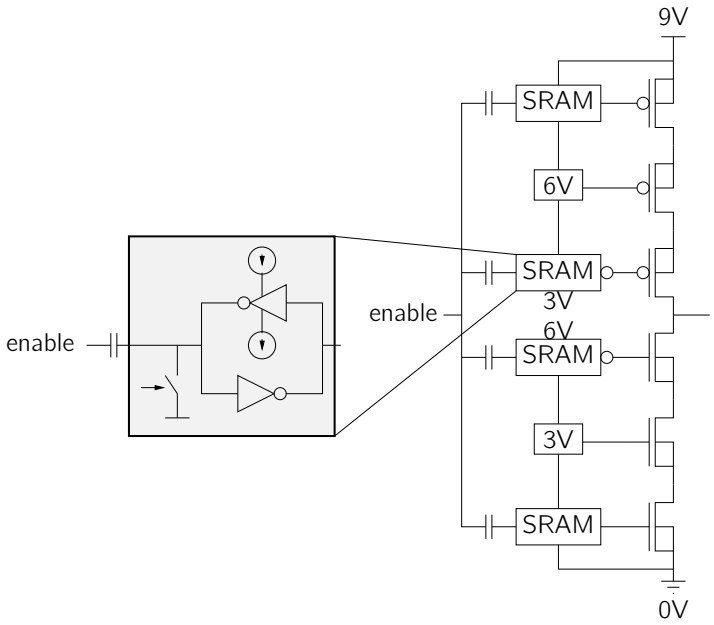

Figure 5.5: Switcher3 block diagram of switch with cap. coupling and storage cell.

$47pF$ capacitor for frequencies greater than $65MHz$ is caused by the transistor's output resistance. The capacitor cannot be charged to $9V$ within a clock period. The power consumption is dependent on the connected load and switching frequency and can be calculated with $I = f \cdot C \cdot U$. A $22pF$ load with additional $\approx 6pF$ parasitic load of the PCB traces and a frequency of $100MHz$ gives $I = 100MHz \cdot 28pF \cdot 9V = 25.2mA$, which matches the measured value. This demonstrates that the chip internal dissipation is negligible with respect to the power required to charge and discharge the gate and clear lines.

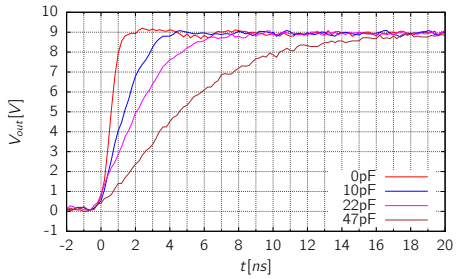

Figure 5.6: Switcher3 measured rising edge for different load capacitors at $9V$ output voltage.

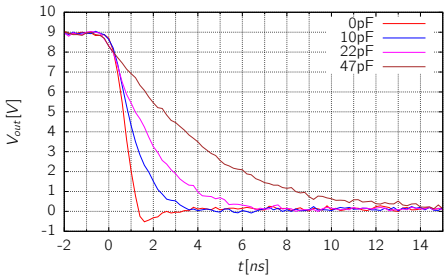

Figure 5.7: Switcher3 measured falling edge for different load capacitors at $9V$ output voltage.

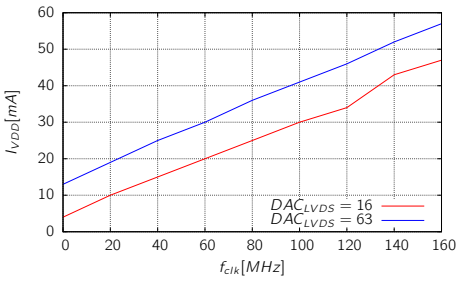

Figure 5.8: Switcher3 measured dynamic digital power consumption.

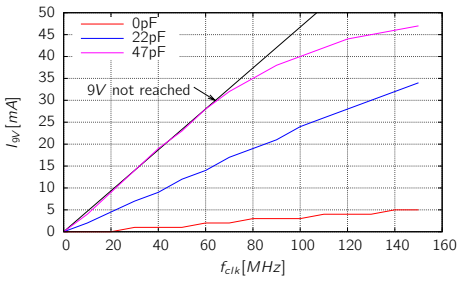

Figure 5.9: Switcher3 measured dynamic analog power consumption.

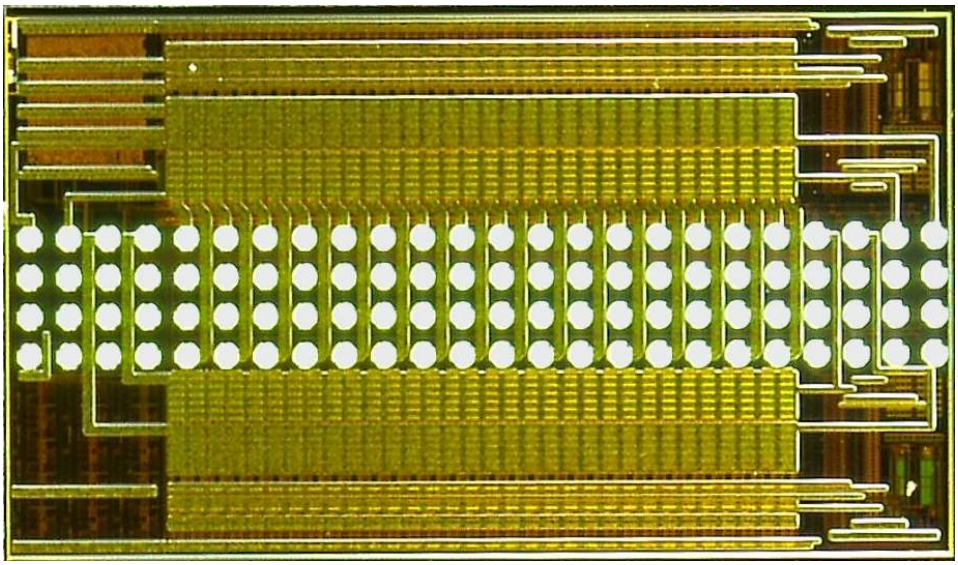

Figure 5.10: Photograph of the Switcher-B die.

5.2 Switcher-B for Belle II

The Switcher-B has been developed to meet the detector requirements of the Belle II experiment. Irradiations of the DEPFET matrix with a thick gate oxide showed a threshold voltage shift of $\approx 20V$, which would significantly exceed the Switcher3's operating range. The use of high voltage transistors with a maximum operation voltage of $50V$ is therefore needed. Radiation hardness is assured by the use of a technology option providing mixed oxide thicknesses for these high voltage transistors. The Switcher-B includes two outputs per channel, but less channels than the Switcher3, due to space limitations on the module balcony.

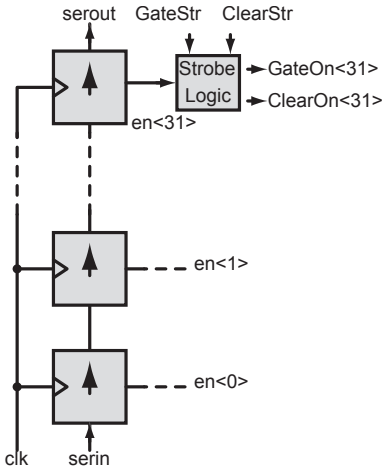

Figure 5.11: Block diagram of the Switcher-B channel selection logic. [42]

5.2.1 Architecture and Design

Figure 5.10 shows a photograph of the Switcher-B with a size of $3600\mu m \times 2030\mu m$. Four rows of bump pads are located in the middle of the chip. This makes the routing on the module balcony more easy. The fan-out of gate and clear signals on the module is on one side of the bump pattern, while the wide power buses are located on the other side. Four bump columns at both ends of the Switcher footprint are used for control signals and power supply. They are placed at the ends to make a series connection of multiple Switcher chips along the DEPFET module's balcony easier. The remaining columns are the 64 outputs: 32 channels with 2 outputs each. The logic cells are located in the corners of the die and the big output transistors at the top and the bottom of their corresponding output pad column.

The output channels are sequentially addressed by a shift register, with its input and output connected to pads to daisy chain the chips along the module balcony. Using a shift register is an easy and safe approach. It is not very sensitive against single event upsets, because there is no data stored. The DHP's logic for steering the Switchers can be much simpler than with the sequencer approach of Switcher3. Once a channel is enabled by the shift register, two strobe signals are used to control the output switches and the edge timing of the gate and clear outputs (see figure 5.11). The strobe logic block allows three operation modes depending on the relative position of the gate strobe signal with respect to the shift register's clock signal:

overlapping The gate signal of the next row is enabled before the current row is switched off. The rising edge of the gate strobe has to occur *before* the falling edge of the clock. The amount of overlap is equal to the time between the rising edge of the strobe and the falling edge of the clock signal. The gate output is switched off with the falling edge of the clock (see figures 5.12 and 5.13).

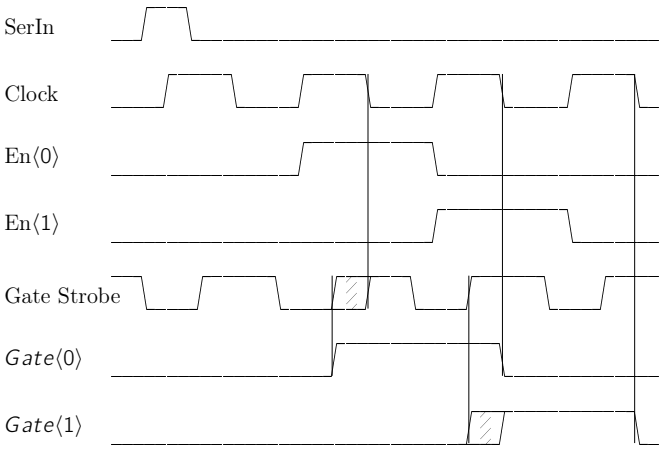

Figure 5.12: Example of overlapping gate strobe timing.

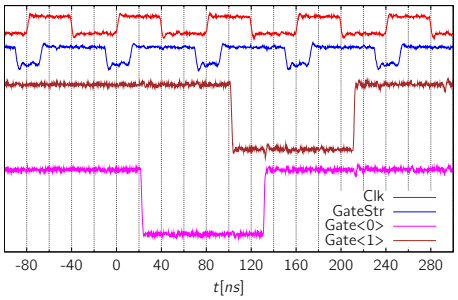

Figure 5.13: Switcher-B measured overlapping gate signals.

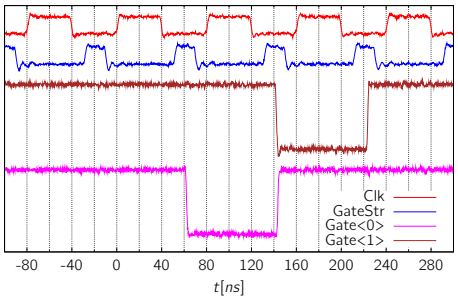

Figure 5.14: Switcher-B measured non-overlapping gate signals.

non-overlapping The gate signals of neighboring rows don't overlap. The rising edge of gate strobe has to occur *after* the falling edge of the clock. The gate output is switched off as soon as the next gate is switched on (see figure 5.14).

skip Rows can be skipped. Their output state doesn't change if the strobe signal is omitted.

The digital core and JTAG voltages can be shifted relative to the output voltages. This allows a flexible operation and output voltages can be adapted to matrix threshold shifts. Figure 5.15 shows the floating and fixed supply voltage ranges. The substrate has to be connected to the lowest potential and the reference voltage for the level shifters must be 3.3V above substrate potential. The digital ground and the low output voltages can be floating. The high output voltages have to be at least 7V higher than their corresponding low voltage and higher than the digital supply. The absolute maximum voltage must not exceed 50V.

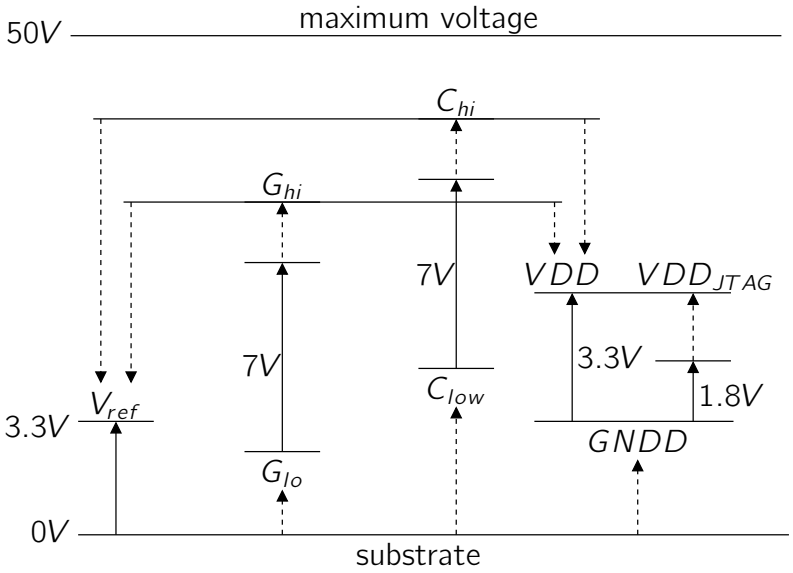

Figure 5.15: Switcher-B floating and fixed supplies voltage ranges.

5.2.2 JTAG

An industry standard JTAG interface has been integrated into the Switcher-B for configuration and debugging purposes. It allows configuration of the bias DACs and access to the boundary scan chain. Boundary scan is a method of sampling and overriding input and output signals of chip steering signals. It could be used to check connectivity of the flip-chip bonding or to test chip functionality prior mounting with a minimum of necessary connections. Figure 5.16 shows the block diagram with the boundary scan chain interfacing the i/o signals and the chip core signals on the right and the JTAG control signals on the left. To be compatible with the $1.8V$ signal levels of the JTAG master on the DEPFET module and the $3.3V$ core voltage of the Switcher, level shifters have been introduced. The JTAG controller has been tested and is fully working.

5.2.3 Output Stage

The output stage of the Switcher-B uses high voltage transistors with two gate thicknesses. The thin part of the gate oxide is located at the source and can withstand $3.3V$, while the thick oxide faces towards the drain and allows $50V$ operation (see figure 5.18). Additionally, these transistors use the enclosed design to reduce radiation induced leakage currents.

Two level shifters are needed to supply the HV transistors with the appropriate gate voltages (see figure 5.17). They use the current based approach and contribute to the static power consumption. A boost mode is implemented to reduce the heat generation: A higher current is flowing when a level shifter is switching, while a reduced current

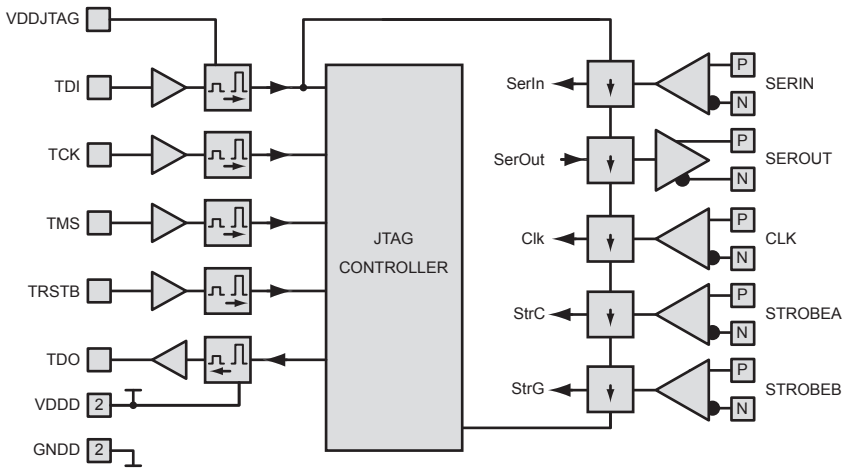

Figure 5.16: Block diagram of the Switcher-B JTAG controller and boundary scan chain. [42]

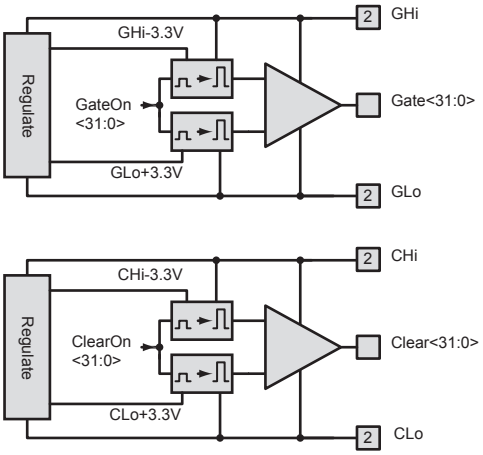

Figure 5.17: Block diagram of the Switcher-B output driver[42]

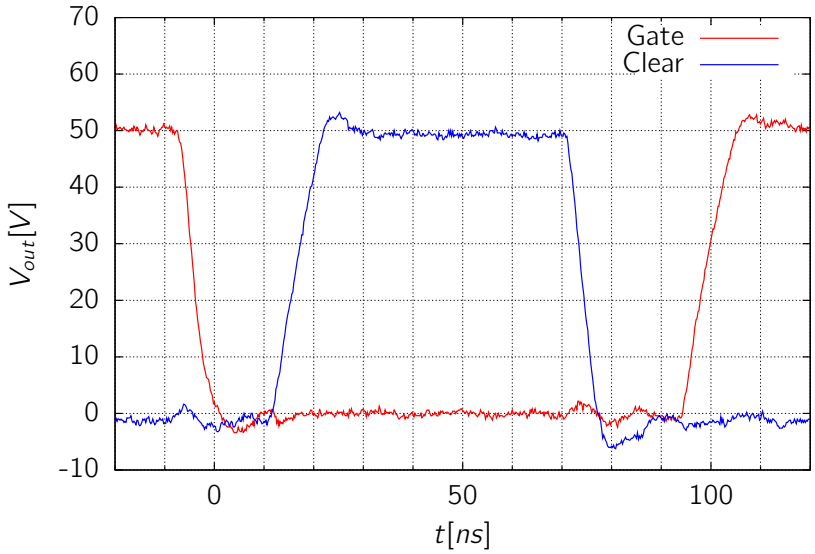

Figure 5.18: Switcher-B measured gate and clear outputs at $50V$ swing.

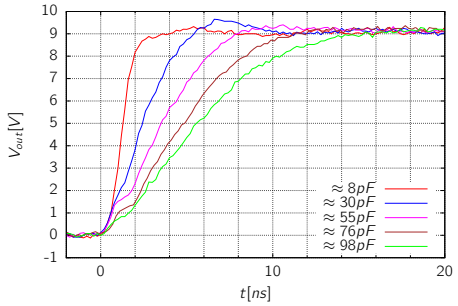

Figure 5.19: Switcher-B measured rising edge for different load capacitors at $9V$ output voltage.

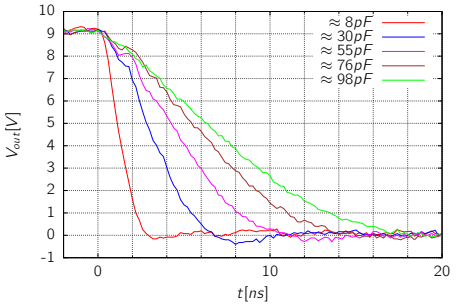

Figure 5.20: Switcher-B measured rising edge for different load capacitors at $9V$ output voltage.

is used to keep static levels. The shift register enable signal boosts the previous, the currently enabled and the next channel. All other channels are in sleep mode.

The rise times of the outputs have been measured for different load capacitors and are shown in figures 5.19 and 5.20. Parasitic extractions based on the PXD6 DEPFET designs show a capacitance on the gate line of a 768 column matrix of $35pF$ [43]. For the final matrix size with 1000 columns the load capacitance can be estimated to $\approx 50pF$. The Switcher-B is capable of charging this load within $10ns$, which is sufficient for the $100ns$ row readout time of the Belle II experiment.

The power consumption on the digital supply and return paths as a function of the clock frequency is shown in figure 5.21. The higher return current is caused by the level shifter circuit, which provides a current path from analog supply to digital ground. Figure 5.22 shows the static power consumption as a function of the bias DAC setting for the boosted channels. This setting has also an effect on switching speed as shown in figure 5.23.

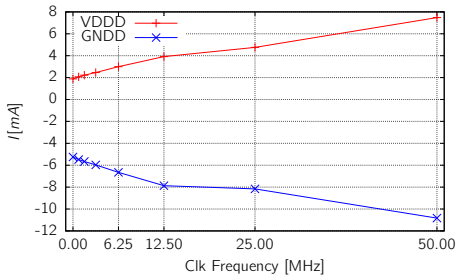

Figure 5.21: Switcher-B measured dynamic digital power consumption.

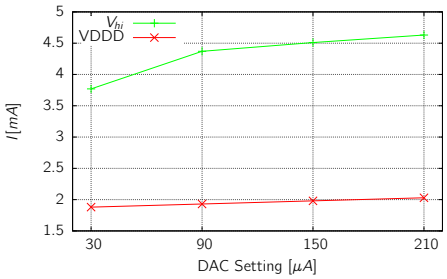

Figure 5.22: Switcher-B measured static power consumption.

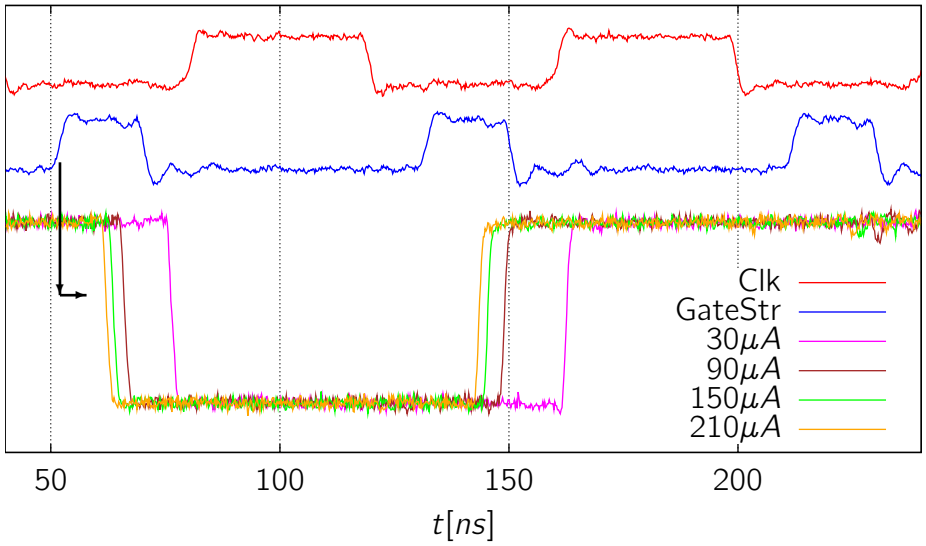

Figure 5.23: Switcher-B measured gate strobe to output delay for different boost DAC settings.

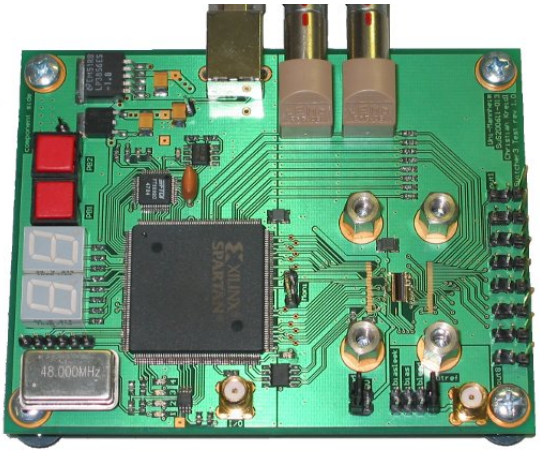

Figure 5.24: Photograph of the Switcher3 test setup.

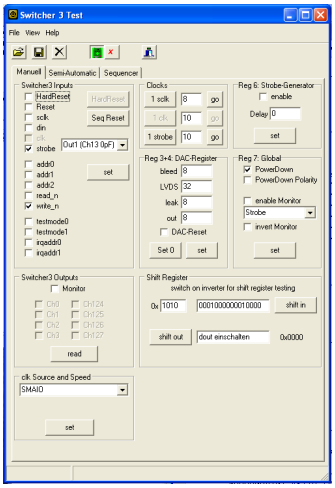

Figure 5.25: Screenshot of the Switcher3 test software.

5.3 Test Setups

Several test setups for characterization and irradiation tests have been developed during this thesis. They are designed to operate the chips standalone, without the other devices of a DEPFET system.

The test PCB for the *Switcher3* shown in figure 5.24 includes an USB interface, a FPGA and a programmable clock generator. The chip can be clocked at up to $200MHz$ and is wire bonded to the PCB. All digital signals are connected to the FPGA. Some output channels are connected to test points with different load capacitors for timing measurements, others are connected to load capacitors only for power consumption tests. A few are connected to the FPGA to automatically test the sequencer. The software shown in figure 5.25 includes several operation modes. Every signal of the chip can be set and read independently in the manual mode. A semi-automatic mode allows testing of the chip registers and RAM with random patterns. The sequencer mode compiles a program and uploads it to the chip.

A PCB design for the Switcher-B has been developed and extends a previously designed test PCB for the DCDB. The board does not contain a FPGA, but connects to the existing FPGA board used in the DEPFET read-out system. As with the Switcher3, the design goal is a high flexibility for debugging. Although the Switcher-B was designed for flip-chip only mounting, wire bonding was possible and all digital signals and some output channels could be connected (see figure 5.26). The software allows for manual control of the steering signals, as well as an automatic mode, which generates the strobe signals. Their position relative to the clock edge is programmable to test the three strobe modes. An automatic measurement mode controls power supplies and the oscilloscope reading and is used for sampling the device's state at regular intervals during an irradiation.

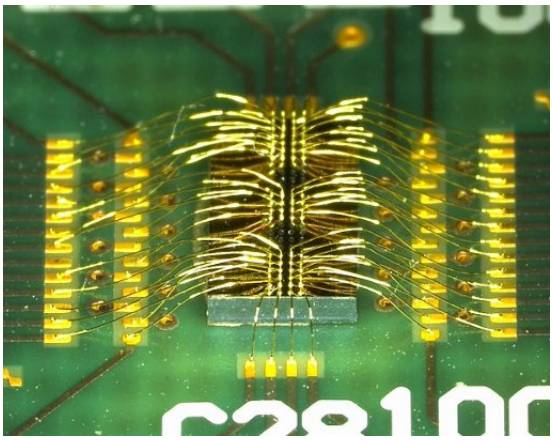

Figure 5.26: Photograph of the Switcher-B wire bonding.

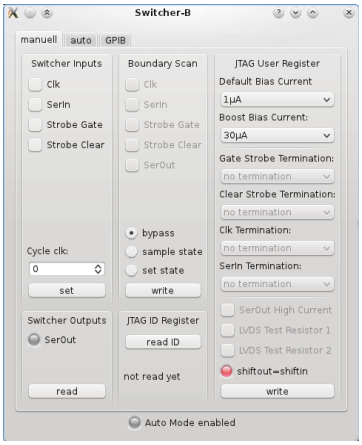

Figure 5.27: Screenshot of the Switcher-B test software.

5.4 Switcher3 Irradiation

The Switcher3 has been irradiated with X-rays (60kV 33mA) up to 10.6Mrad[2], with a dose rate of 113.7krad/h. It was fully biased and running during the irradiation, with a small sequencer program cycling between two channels. A dose of 10Mrad has been chosen to be able to see effects in the radiation hard design. An accumulated dose of only 200krad in 5 years is expected at the ILC for the chips on the innermost detector layer. Measurements of the channel outputs had to be taken manually, whereas the supply currents were measured automatically every hour. Channel measurements have been taken at doses of 0Mrad, 2.7Mrad and 10.7Mrad.

The first measurements after 2.7Mrad showed a wrong switching pattern at 100MHz clock frequency (figure 5.28). In the first two loop cycles, the second command is delayed by one clock. The correct sequence is recovered by reducing the speed to 50MHz (figure 5.29). This can be explained by an increased propagation delay of the destination jump address, causing setup time violation in the address register. The signals have settled at the next clock edge and the program continues at the next command. Other errors show no active or two simultaneously active channels. This can be caused by propagation delay of the asynchronous channel decoder, which creates an one-hot encoded signal from the 7 bit channel address. Long buses are distributing signals in the asynchronous path across the chip to all output drivers. Buffers weakened by irradiation cannot change the capacitive load fast enough and the registers in the output channels sample a wrong state.

Figure 5.30 shows the outputs at a dose of 10Mrad at 10MHz. The state changes are asynchronous to the clock signal and could be caused by the strobe signal or a flipping

[2]Dosimetry provided by the irradiation facility was wrong at the time of irradiation and is here corrected by a factor 0.47. [44]

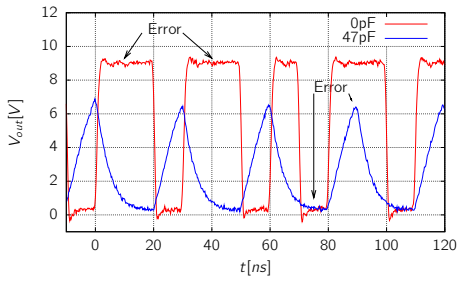

Figure 5.28: Switcher3 at $100MHz$ after 2.7Mrad irradiation.

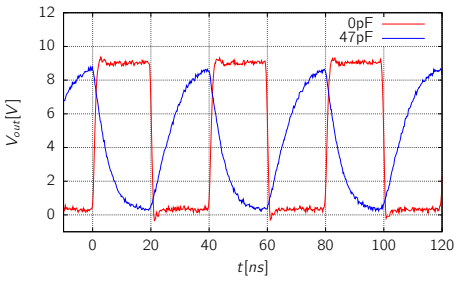

Figure 5.29: Switcher3 at $50MHz$ after 2.7Mrad irradiation.

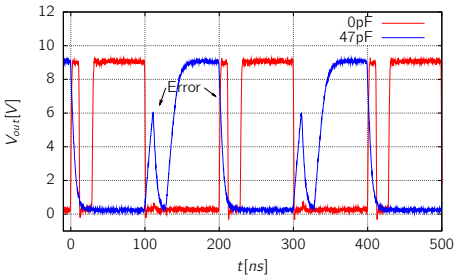

Figure 5.30: Switcher3 at $10MHz$ after 10.7Mrad irradiation.

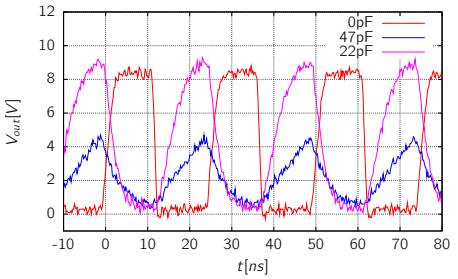

Figure 5.31: Switcher3 at $80MHz$ after 40 days annealing.

memory cell of the capacitive coupling.

The rise times double at a dose of 2.7Mrad (figure 5.32) and increase to $17ns$ for the $47pF$ load. As expected, the radiation induced effects recover after annealing due to tunneling or thermal excitation processes. The rise and fall times get close to the 2.7Mrad values after 40 days annealing at room temperature. The output timing for the expected ILC matrix load of $\approx 20pF$ are $t_{rise} = 6.5ns$ and $t_{fall} = 4.2ns$. An operation at $80MHz$ is possible with a full $9V$ swing output signal and without sequence errors (figure 5.31).

Figure 5.33 shows the supply current of the digital and analog supply as a function of the dose. The large drop of supply current at a dose of 2.5Mrad is caused by a reduction of clock frequency. The chip was running at $150MHz$ and could not fully charge the load at the output due to the radiation damages in the output drivers. Timing analysis were not possible until reducing the clock frequency to $50MHz$ and thus restoring the full $9V$ swing at the output.

The Switcher3 can be considered as radiation tolerant for the expected dose of a few hundred krad at the ILC inner layer module. Even after 10.7Mrad irradiation and 40 days of annealing it is capable of reaching the goal of charging a $22pF$ load to $9V$ in less than $10ns$.

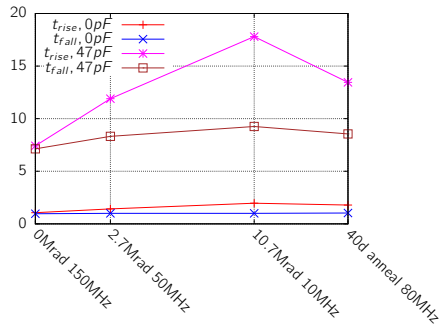

Figure 5.32: Switcher3 edge timing as function of dose.

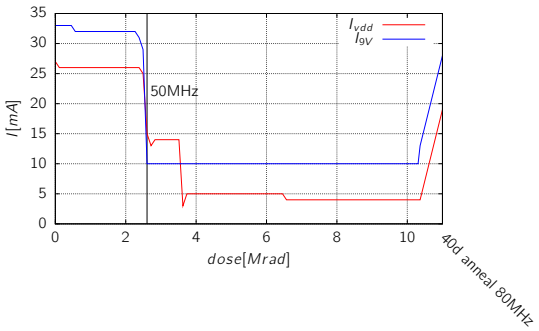

Figure 5.33: Switcher3 supply currents as function of dose.

5.5 Switcher-B Irradiation

The chip has been irradiated with X-rays (60kV 33mA) with a dose rate of 636krad/h up to an accumulated dose of 24.5Mrad. The chip was running at 12.5MHz during the irradiation and was cycling through output channels. Timing measurements were taken at channels connected to 76pF load.

Figures 5.34 and 5.35 show the gate and clear outputs for different doses and after annealing. The falling edges of clear and gate behave differently. A by 7ns decreased speed of the gate output can be observed at a dose of 24.5Mrad, whereas the clear speed increases by 5ns. This asymmetry can only be caused by the control logic generating the steering signals for the output drivers because the same output drivers are used for the gate and clear outputs. The gate control signal is generated by an or-gate and is not buffered, while the clear signal is buffered. The rising edges of gate and clear are slower by 2ns and 3ns, respectively. Figure 5.36 shows a summary of the edge timings. The supply current increases within the first 500krad from 5mA to 35mA on the digital supply and doubles on the analog supply. It recovers to the pre-irradiated state at a dose of 7.3Mrad (figure 5.37). This behavior has also been observed on other chips and could be caused by different effects of NMOS and PMOS devices.

With a dose rate of 2Mrad/year and 5 years of operation in Belle II the Switcher-B would suffer a falling gate edge decrease by 3ns whereas the clear edge increases speed by 5ns. Changes of timing can be less, as annealing effects can reduce the irradiation damages caused by the low dose rate instantly. The desired row readout speed of 100ns can be reached with this chip and it can be considered radiation hard.

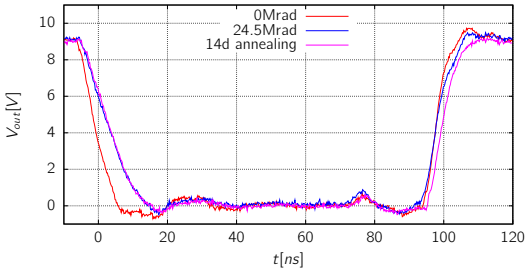

Figure 5.34: Switcher-B gate output at different doses and after annealing.

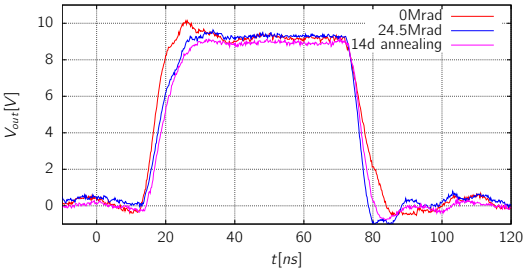

Figure 5.35: Switcher-B clear output at different doses and after annealing.

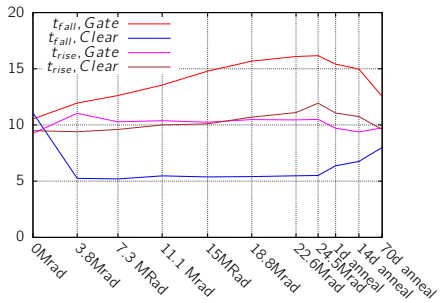

Figure 5.36: Switcher-B edge timing.

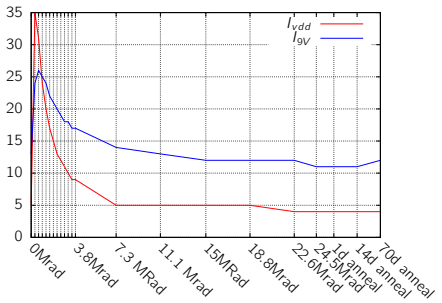

Figure 5.37: Switcher-B supply currents as function of dose.

6 Interconnection Technology Developments

The semiconductor interconnection technology developments are mainly driven by the commercial mass production. It created cost effective processes, which allow bonding of high pin count devices within a minimum of time. Some of these technologies allow processing of single die, while others are only available on a wafer level.

Chip productions in research and development are often based on multi-project submissions, where designs from multiple customers are collected and manufactured with one wafer mask set, distributing the setup costs to all customers. The wafers are diced and each customer receives a small amount of *single* dies. Some multi-project vendors offer wafer level interconnection processes, but for other chip technologies single die interconnection methods have to be used, as uncut multi-project wafers cannot be ordered. Single die processing for technologies like flip-chip bumping is uncommon in industry and can rarely be ordered commercially, especially for the low volume needed in research and development. Commercial single chip bumping is expensive and bumping itself was less common at the start of the ILC detector developments.

Multi-project wafer productions were used for the ILC and Belle II chip developments. The interconnection methods evaluated in this thesis were chosen with respect to the single die processing capabilities, the ability to operate them in the existing environment and the flexibility to adopt to different chip designs easily.

6.1 Wire bonding

Wire bonding is one of the basic technologies used in the semiconductor industry. It is very flexible and can be used in a wide range from prototyping in research and development to mass production.

In wire bonding technology, a round wire is used to form the electrical connection between the silicon chip and the substrate. The wire materials commonly used are aluminum, gold, copper or palladium. Wire diameters from $13\mu m$ to $500\mu m$ are available and used from low pitch up to high current applications. It is distinguished between two bonding processes: the ultrasonic wedge/wedge and thermosonic ball/wedge process.

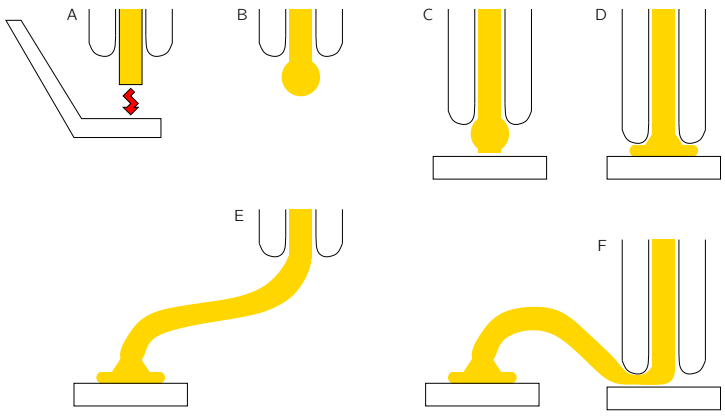

Figure 6.1: Ball/Wedge wire bonding steps with ball flame-off (A+B), ball bonding (C+D), loop forming (E) and wedge bonding (F).

A bonding tool with a flat, rectangular foot is used in the wedge/wedge process to press the wire onto the pad. Ultrasonic energy is then applied to the bonding tool to form the mechanical and electrical bond connection. This process is mainly used for aluminum, rarely for gold wires. It is called wedge/wedge bonding, because the source bond on the chip and the destination bond on the substrate are both created with the same technique.

A different type of tool and a slightly different process is used for the ball/wedge bonding. Figure 6.1 illustrates the process: The bonding wire is fed through a round capillary, made of ceramic material, and ends shortly after the capillary's tip. A high voltage spark or a flame is used to melt the end of the wire ('flame-off') causing it to form a ball by its surface tension (A). The diameter of the ball can be adjusted by the current and duration of the high voltage spark. The inner diameter of the tip's hole is only slightly larger than the wire and prevents the ball from entering the capillary. Vacuum pulls the ball towards the tip and centers it in the inner chamfer (B). Then, the bond tool presses the ball onto the bonding pad (C) and ultrasonic energy is applied to scrub the ball to the pad and to form the bond (D). The bonding machine then moves the capillary to the destination position on a defined vertical path to form a wire loop (E). The wire is pressed to the pad at the destination where it is wedge-bonded to the substrate (F). The wire is flattened during bonding, which allows to rip it off without destroying the bond. The substrate has to be heated to $120 - 200\,^{\circ}\mathrm{C}$ to support the formation of the metallurgical connection.

Aluminum bonding benefits from lower wire prices and allows processing of temperature sensitive devices. Low bonding pitches can be achieved for parallel bonds, but low bonding pitches with high angled wire fan-outs can cause short circuits. The wedge bond has to be rotated in direction of the destination pad to prevent wire breakage near the bond (neck breakage). A short circuit is created if the end of the rotated wedge bond touches the neighbor pad. Aluminum wedge/wedge bonding is predominant in R&D sensor labs. Ball/wedge bonds are created faster, because the bond tool doesn't need to be rotated

in direction of the bond. It has a lower resistivity than aluminum and can provide equal electrical performance with thinner wires. Copper wire is cheaper than a gold wire, but needs an inert atmosphere during bonding to prevent oxidation, especially for the flame-off.

6.2 Flip-Chip Bonding

The flip-chip bonding process offers advantages over the wire bonding connection, such as a lower area requirement, shorter paths between substrate and chip, lower inductance and a fast parallel bonding process. The pads of substrate and chip are placed face-to-face and brought into contact using a conductive material. Flip-chip bonding needs less area on the substrate, because the landing pads are covered by the chip, whereas wire bonding needs space for wire looping and for the destination pads located around the chip. The path between source and destination pads is only a few tens of micrometers long, whereas bonding wires are in the range of hundreds or thousands of micrometers.

Different conductive materials can be used to form the interconnection, e.g. gold-stud bumps, solder bumps, indium bumps or conductive glues and films. Gold-stud bumps can be easily placed with a modified wire bonder, but require high bonding forces in the range of 40-60gr/bump and temperatures up to 320 °C. Indium can be bonded with 60 °C and <10gr/bump, but the bumps are deposited by evaporation, which needs additional preprocessing. Solder bumps can be deposited in many ways (see chapter 6.4), including a flexible single ball placement. Solder processing parameters range between those of gold and indium bumps. Glues and foils share the advantage of supporting the mechanical stability of an assembly by their adhesive properties. They require lower temperatures and forces for curing the adhesive, but have a higher resistivity and require larger pads and pitches.

Thermocompression, thermosonic, soldering or curing processes are used form the bonds after aligning the pads of chip and substrate. A high temperature and force is applied to form the bond at thermocompression bonding. Thermosonic bonding utilizes ultrasonic energy to reduce the force. In soldering processes, the pads are joined by temperature only. Additionally, fluxes or inert atmospheres have to be used to assist solder joint forming. Heat or UV-light is common for curing glues and films. [45]

High energy physics detector developments benefit from the flip chip bonding, as it allows a compact module design with dense packaging and a low material budget. The goal of the flip-chip developments in this thesis is the creation of a novel all-silicon module, where read-out and steering chips are flip-chip bonded directly to the detector silicon, without the use of any interposers like PCB, ceramics or kapton cables. The all-silicon approach gives a compact module, with a minimum of material added to the active area and the benefit of the same thermal expansion coefficients of substrate and chips. This reduces stress to the chip interconnections during operation and thus reduces failures.

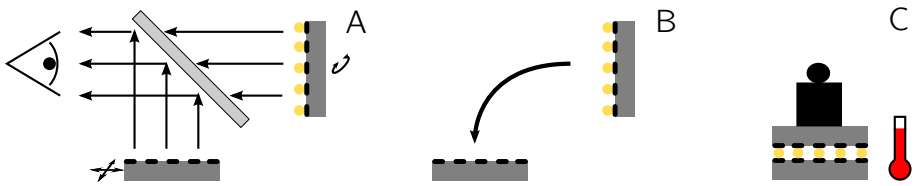

Figure 6.2: Flip-chip process with alignment, placement and thermocompression bonding.

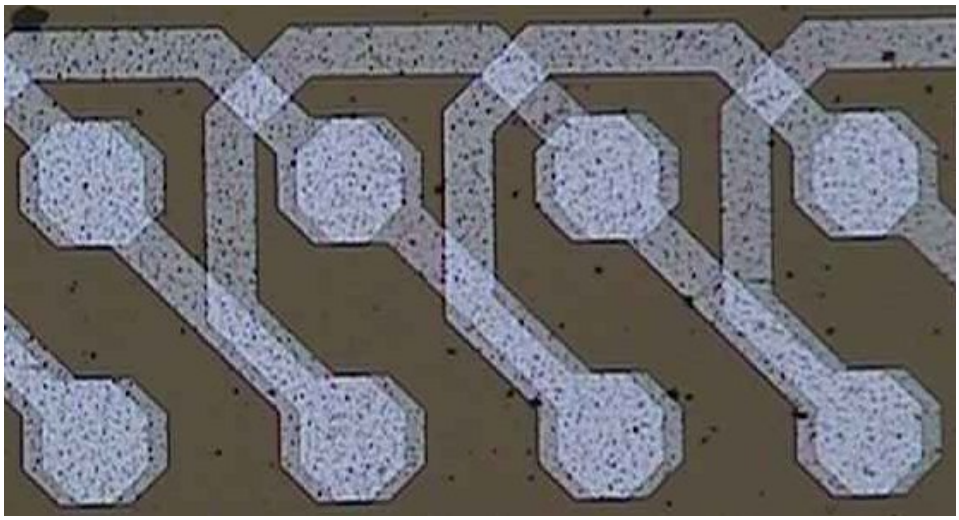

Figure 6.3: Superimposed image of Switcher3 dummy-chip and substrate. They are aligned vertically, but unaligned horizontally.

The interconnection material can also assist in chip cooling, as it transfers heat from the chips to the cooled module.

The flip-chip process starts by picking up the chip with a bond tool and placing the substrate on the bond table. Chip and substrate pads are then precisely aligned. The bond tool places the chip onto the substrate, while maintaining the precise alignment. The bonding is performed by applying a defined pressure while cycling through a temperature profile. Fully automatic machines for mass production use camera systems with pattern recognition to pick up and align the devices. The machine used during this thesis is a manual machine for R&D, reworking or low volume productions. Pick up, alignment and chip placing is a manual process, while the temperature profile is automatically cycled.

The manual process in the 'Fineplacer Lambda' is depicted in figure 6.2. The substrate is placed on the table and the bumped chip is fixed on the bond head by vacuum. An optical beam splitter superimposes the two images of the chip and the substrate to visualize the relative position of pads and bumps (A). The substrate is moved horizontally and the chip is rotated by the operator, until the pads and bumps are aligned. The chip is placed on the substrate in a precise 90° movement, maintaining the aligned position (B). The desired force is applied and a temperature cycle is started to form the bonds (C). Temperatures

Figure 6.4: Photograph of bumps with long tails caused by non uniform rip-off of the $25\mu m$ wire.

of up to 400 °C with a gradient of 20K/sec and forces of up to 400N can be applied and allow thermocompression bonding and soldering of assemblies with a placement precision of $0.5\mu m$.

6.3 Gold-Stud Flip-Chip Bonding

Gold spheres are used in gold-stud flip-chip bonding as interconnection material between chip and substrate. These sphere are called gold-studs and are produced using a modified wire bonding process. A gold ball is bonded to the pad like in the ball/wedge wire bonding, but instead of forming a loop the wire is ripped off as close as possible to the ball.

A benefit of the gold-stud bumping is the flexible process derived from wire bonding, which can be easily adopted to different chip layouts and connection counts. It doesn't need different mask sets, chemical processes for bump deposition or under bump metallizations. The sequential bump placement is slower than parallel wafer-bumping processes, but it allows bumping of single chips easily. In multi-project wafer productions it is often not possible to request un-diced wafer for wafer-level bump processing. Many commercially available bumping technologies can only process on a wafer scale.

Multi-project wafer productions have been used in the development of steering and read-out chips for the ILC. Unfortunately, they didn't offer access to wafers or wafer-lever bumping processes. This necessitated the use of a single chip capable bumping process, that was installed and operated in the available facilities.

The first bumping tests have been made with a $25\mu m$ diameter wire on a manual bonder. The wire was of a type that had been normally used for ball/wedge bonding. It was made of a softer gold alloy with an elongation of 2-6% and a break load of >7cN and showed a

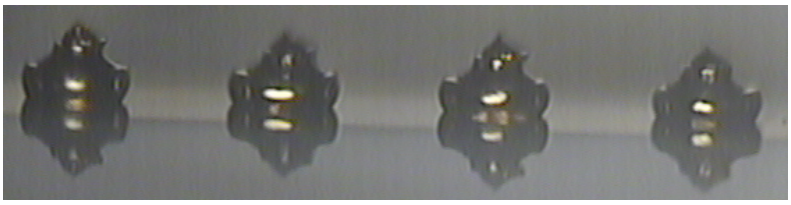

Figure 6.5: Photograph of bumps with uniform and short tails.

Figure 6.6: 48μm free air ball on 17.5μm wire.

non-uniform rip-off at gold-stud bumping. Figure 6.4 shows 65μm diameter test bumps with about $60-120\mu m$ long wire tails. These tails can cause shorts to neighboring bumps during flip-chip bonding, as they possibly bend sidewards and touch neighboring bumps. A uniform bump height with short tails is desired to avoid shorts and to ensure that every bump is in contact during flip-chip bonding. Larger free air balls showed a more consistent tail length, but bump diameters of 120μm were not acceptable for bumping on the Switcher3's pads with 80μm diameter and a pitch of 100μm. Small balls resulted in a weak bumping performance, where bumps were not bonded at all or were removed by the wire rip-off. This is explained by the low volume of the gold ball, which has to fill the bond capillary's inner chamfer in order to transmit the ultrasonic power to the bond interface correctly.

The tail length is influenced by the heat affected zone, which corresponds to the part of the wire which is heated, but not melted during the flame-off process step. The grain structure is coarser in this zone, due to the influence of the heat and the wire is more vulnerable to shearing stress. The stiffer wire assists automatically with high loop forming, but can break close to the ball during low loop bonding. A short heat affected zone is desired at bump bonding, to reduce the tail length. The size of the heat affected zone can be reduced by doping or alloying the pure gold, e.g. with beryllium [46].

A harder wire with 17.5μm diameter and an elongation of only 0.5-2.5% with a break load of >8cN was used next, together with a capillary optimized for bumping. This capillary has a flat tip to direct more ultrasonic energy to the ball bond, because it doesn't need to provide the wedge bond capability. The wire performed better, with short and uniform tails. Another approach to control the tail length has been tested as well: The wire is sheared of by a sidewards movement of the capillary closely to the ball. This removes a part of the ball's tip and creates a flat surface. But the shearing also bends the wire end, which then gets stuck in the capillary more often and interrupts the bumping process. The tail length can also be controlled by multiple horizontal capillary movements close to the bump, which bends the wire in the heat affected zone. This bending weakens the stiffer heat affected zone and the wire can rip of easily. A more uniform tail length was

observed with the softer wire, but the bending is unnecessary with the harder bumping wire. It slows down the process and causes the wire to get stuck, too. The simple vertical wire rip-off results in a better process flow.

Figure 6.5 shows bumps produced with the harder wire. They have a diameter of $60\mu m$ diameter and $40\mu m$ height. $10\mu m$ short and uniform tails can be seen on all four bumps. Figure 6.6 shows a free air ball (FAB) with a $48\mu m$ diameter at the end of the $17.5\mu m$ diameter wire, created by the flame-off process.

6.4 Solder Bump Flip-Chip Bonding

Flip-chip assembly with solder bumps has many advantages over the gold stud method. The chips can be bumped on a wafer scale, which is a fast parallel process compared to sequential gold stud bumping and is time-saving in mass production. The solder bumped chips can be assembled without high forces, they are placed onto the substrate and heated to melt the solder. This is a benefit for the Belle II DEPFET modules, where the balcony will be partially thinned and wouldn't withstand high forces. Soldering is done by cycling a temperature profile with relatively low temperatures. The melting point of about 220 °C is only reached for a short period of time. The thermal stress to devices is much higher with thermocompression bonding, as the high temperature is constantly applied and might affect the doping profiles of the detector. The melted solder causes a self-alignment of the device to the substrate and makes high precision placement unnecessary, thereby saving time in chip alignment and equipment costs. As solder can be remelted, it allows the replacement of damaged chips and saves precious DEPFET detectors.

A solder wettable surface like copper or nickel is needed to place solder bumps on. Most semiconductor technologies provide only a wire bondable surface with an aluminum finishing. As aluminum is not solder wettable, it needs to be covered with different metal layers. This layer build-up is called under-bump-metallization (UBM). The different layers consist of metals with good electrical and mechanical adhesion to the aluminum, which are wettable by solder and a layer that protects from oxidation. Applying the commercially used UBM types to single chips is difficult, since these are also optimized for wafer level processing. [47] [48]

6.4.1 Wafer Level Bumping

Industrial solder bumping is mainly a wafer level process, as it is developed for mass production. It is often not available for R&D projects using multi-project wafer productions. Some companies offer solder bumping for multi-project productions as an option to the standard, wire bondable chip surface.

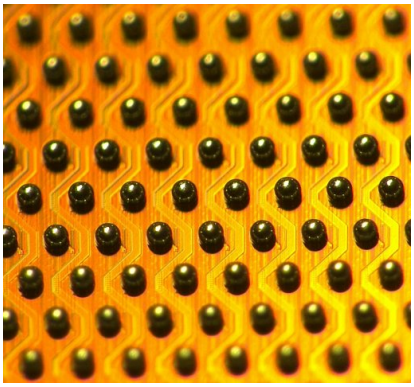

Figure 6.7: Photograph of the DCDB solder bumps with $100\mu m$ diameter and a horizontal pitch of $200\mu m$ and $180\mu m$ vertically.

Different methods are available for under bump metallization deposition on a wafer level. Metal can be deposited by heating it up until it evaporates and deposits to the wafer. A mask is used to define the positions to deposit to. Another method is sputtering, where material is removed from the metal by ion bombardment. The free metal atoms are deposited on the full wafer area. A photoresist covers the bump positions and the excess metallization is etched away.

Solder can be deposited by either evaporation, electroplating or screen printing. Electrical currents are used in electroplating to deposit the soluted solder to the bump positions defined by a photo resist. The wafer needs to be completely covered by UBM to allow an electrical connectivity to all bump positions. The photoresist and the excess UBM have to be removed after bump deposition. Electroplating can create small bump sizes with a diameter of about $10\mu m$. Screen printing is the cheapest technology and uses a mask to print the solder paste onto the pads. The spherical bumps are formed after removing the mask by melting the solder paste deposits (reflow) in an inert medium. The bump pitches and sizes are much larger due to the limitations of the stencil mask and range between $150 - 200\mu m$ pitch and $\approx 100\mu m$ diameter [49].

A wafer level solder bumping was available for the DCDB production on a multi project submission of the UMC 180nm technology. The offered technology is able to add solder bumps to a wire bond-only chip layout. It therefore includes an additional routing layer for connecting the wire bond pads at the chip edges to the bump pad array in the center. This layer is applied after the normal processing steps and is of rather large feature size. The bump material was chosen to be of the lead-free solder type SAC305, an alloy of 96.5% tin (Sn), 3% silver (Ag) and 0.5% copper (Cu) with a melting point of $\approx 218\,^{\circ}C$. Figure 6.7 shows the DCDB solder bumps with $100\mu m$ diameter and a horizontal pitch of $200\mu m$. The additional routing layer can be seen between the bumps, which connects the bumps and is also used to distribute a supply voltage across the chip.

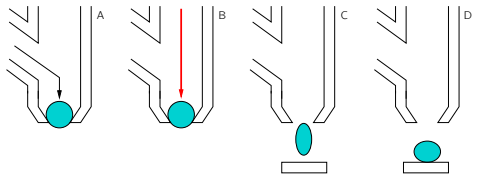

Figure 6.8: Solder jetting process. See text for description.

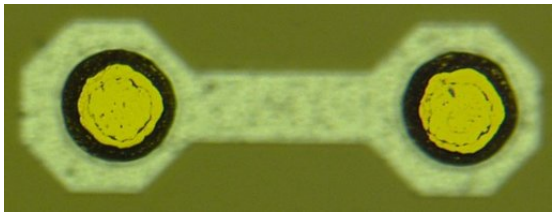

Figure 6.9: Gold stud bump with flat top ready for solder bump placement.

6.4.2 Single Chip Solder Bumping

As some wafer level processes, like screen printing, could in theory be also used for single chips, they are less flexible, requiring mask sets and complex preprocessing. A single solder ball deposition process, using a jetting technique, was found to be optimal to meet the flexibility requirements. It can be installed in the available facilities and is a sequential process with comparable benefits and drawbacks of the gold-stud bumping.

A single chip bumping technology was installed in the local facilities to place solder bumps on devices where a wafer level bumping is not available or the required bump pitch is too small. The solder jetting technology was chosen, because it doesn't need mask sets and can be flexibly adjusted to different bump patterns. It neither needs toxic chemicals for plating, nor solder pastes. The solder is delivered as a powder with single spheres of a controlled diameter. The machine can support sphere diameters from $60\mu m$ up to $760\mu m$. Currently, only the $60\mu m$ diameter balls are in use.

Figure 6.8 illustrates the solder jetting process. The solder balls are stored in a reservoir and singularized by a disk with holes and thickness matching the ball diameter. A single ball is fed into the capillary with an exit hole smaller than the ball (A). It clogs the hole and nitrogen pressure is applied to the airtight bond head. An infrared laser pulse melts the ball in the capillary (B) and the pressure blows the melted solder out (C). It is deposited onto the destination pad and solidifies (D).

This process requires nitrogen gas to prevent the solder balls from oxidizing during the jetting process and during storage in the reservoir. The process can be adopted to different ball sizes by exchanging the capillary and the singularization disc.

An under bump metallization is also required for the solder jetting process. As the devices are delivered with an aluminum pad finish and the standard UBM processes are not available, a flattened gold stud bump is used to place on the solder spheres. The gold bumps are flattened (coined) by pressing a glass plate with a defined force upon the bumps. A force of 40gr/bump creates a flat top with $40\mu m$ diameter on the $60\mu m$ diameter gold bump (figure 6.9). Afterwards, the chip has been solder bumped with $60\mu m$ solder balls, which created bumps with $65\mu m$ diameter and $40\mu m$ height (figure 6.11). Due to the positioning error of the gold stud bump relative to the pad center, the

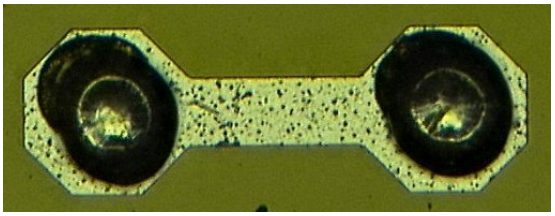

Figure 6.10: Top view of solder bumps on top of gold studs.

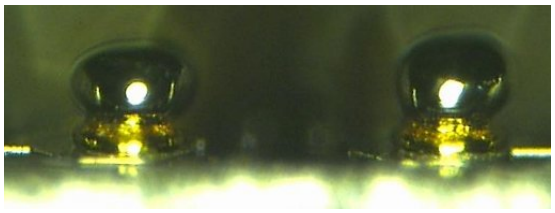

Figure 6.11: Side view of solder bumps on top of gold studs.

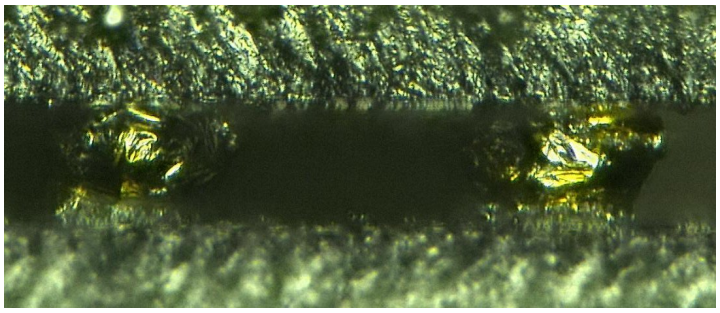

Figure 6.12: Photograph of soldered assembly with gold studs used as an under bump metallization on the chip and on the substrate.

position of the solder on the gold bump is slightly off center (figure 6.10).

The solder balls are of the same material SAC305 as the DCDB bumps, to assure an equal melting point during assembly of a DEPFET module. Figure 6.12 shows the side view of a soldered assembly, where gold stud bumps have been used as an UBM on the chip and the substrate. A soldering cycle starts with a preheat phase of about 120 seconds and slowly heats up all components. The temperature is then increased quickly above the melting point and stays constant for 10-30 seconds in order to form the solder joint. The assembly is then cooled down to ambient temperature.

The same devices have been used for evaluation of the solder jetting process as for the gold-only flipping. The solder bumped chip has been aligned and slightly placed onto the gold studs of the substrate to deform the small gold tails and ensure a contact between gold and solder. The temperature cycle was started after shutting off the vacuum holding the chip. It is observed that the chip slightly moves downwards, when the melting temperature of the solder was reached. The assemblies were measured and showed only one failure in 150 connections.

6.4.3 Reworking of Damaged Assemblies

A benefit of solder flip-chip assemblies, besides the low assembly forces, is the ability to rework damaged chips. Heating a soldered chip to the liquidus temperature of the

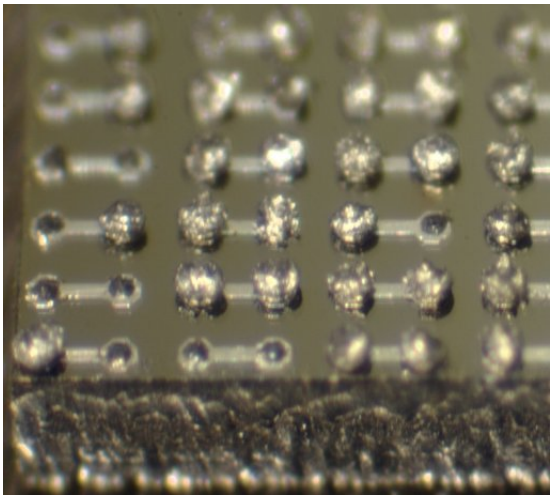

Figure 6.13: Dummy chip after desoldering. Some solder balls remained on the substrate.

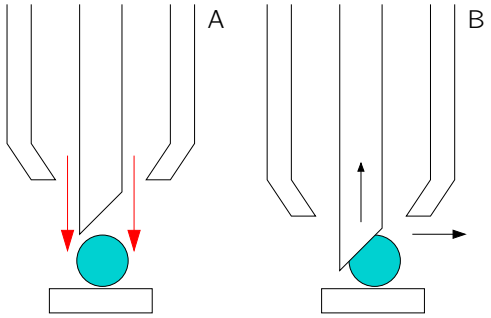

Figure 6.14: Selective removal of solder by melting with hot gas and removing with vacuum.

used solder alloy allows to remove the die from the substrate. Parts of the melted solder remain on the removed chip, while other parts remain on the substrate. Figure 6.13 shows a desoldered dummy chip with $100\mu m$ solder bumps, where some balls remained on the substrate. Soldering a new chip to an uncleaned substrate may cause shorts or unconnected bumps due to the unequal solder volume. The substrate pads have to be cleaned of remaining solder prior soldering a new chip.

The solder jetting machine has been ordered with an additional desoldering head. It allows a selective removal of solder balls. Its working principle is shown in figure 6.14. The substrate is pre-heated to a temperature below the melting point to assist a selective melting of solder balls. The solder ball's temperature is increased above the melting point by hot nitrogen gas blown through a heating nozzle (A). The head moves then downwards and vacuum is applied to the tapered capillary. A sidewards movement pushes the solder ball to the pads edge and the vacuum removes it (B).

6.5 Test Structures

Test substrates and test chips were used for evaluation of the flipping process, which create daisy chain connection of bumps after flipping. The substrate includes multiple pads for probing the connectivity of the daisy chained bump connections. Flip-chip process parameters like pressure, time and temperature were evaluated with gold stud and solder bumps.

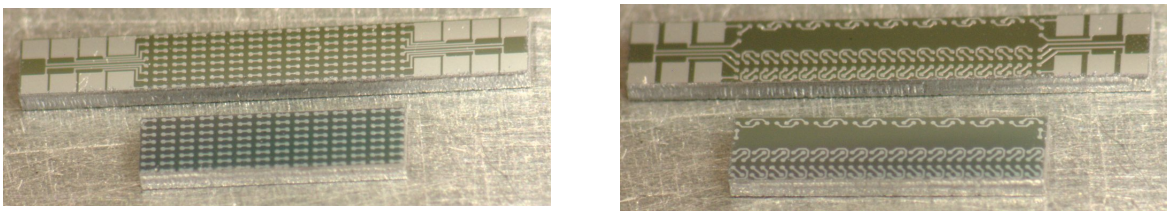

Figure 6.15: Photographs of DCD2 and Switcher3 dummy chips for flip-chip connectivity tests.

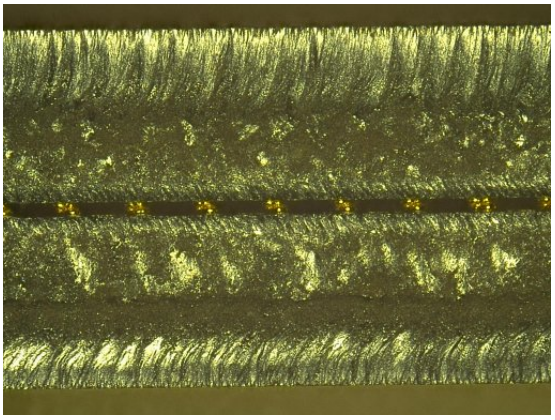

Figure 6.16: Side view of Switcher3 dummy chip with double bumps.

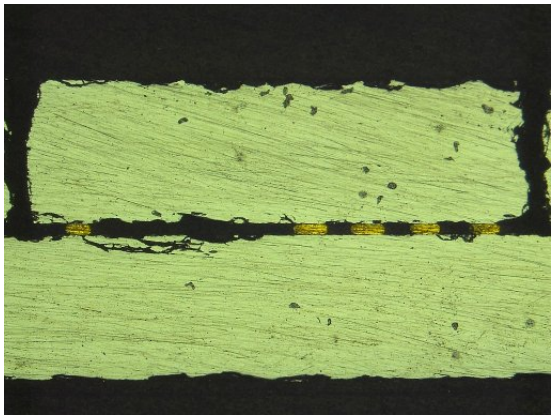

Figure 6.17: Cross-section of Switcher3 with single bumps.

6.5.1 Glass Substrates

The first test vehicles used were made of glass substrates with gold coated structures. They included 4 daisy chain connections of 16 bumps each, with probe pads for connectivity tests. Single bump and double bump approaches have been tested. Single bump assemblies use bumps on the chip only, while bumps on the chip and on the substrate are called double bump. The same flip-chip parameters have been used with all assemblies. A pressure of 80gr/bump and 350 °C for 120 seconds forms the connection during the thermocompression bonding. Both assembly types showed successful bonds on all bumps, determined by the electrical connection. A resistivity of $13\Omega \pm 0.2$ has been measured for all snake structures, which includes the trace resistances. The bond quality has been checked by shearing the chip off the substrate. The bond interface broke equally on the chip and on the substrate side of the bump, indicating that thermosonic bumping and thermocompression flip-chip bonding created equally good bonds.

6.5.2 ILC Silicon Substrates

The gold dummy chips were sufficient for the first test, but the Switcher3 and DCD chips, as well as the DEPFET module are based on silicon substrates with aluminum structures and have a higher pad count. The higher pad count results in a high pressure applied to the chip and substrate, which can possibly cause mechanical defects on the thinned DEPFET modules. A new set of test vehicles has been developed during the thesis, to adopt the bumping and the flip-chip processes to aluminum structured devices. The dummy chips should be mechanically as similar as possible to the real chips, although they were manufactured in a different technology and without active devices. 6“ wafers with a single aluminum layer have been used to produce the test dummies. They were structured with a wafer size mask, which allowed to include a full size ILC module design as a mechanical demonstrator together with the DCD and Switcher dummy chips. They have been manufactured at the MPI semiconductor laboratory, which also manufactures the DEPFET matrices. Layouts for DCD and Switcher3 dummy chips are shown in figure 6.15. The $4960 \times 1350 \mu m^2$ large DCD dummy chip is mounted on the $9545 \times 1350 \mu m^2$ large substrate forming 8 daisy chain structures with 28 bumps each and a total of 224 connections. The Switcher3 chip has a size of $5790 \times 1540 \mu m^2$ and is forming 6 daisy chains with up to 32 bumps and a total of 164 connections, when bonded to the $9546 \times 1350 \mu m^2$ large substrate.

Flipping the silicon dummies with aluminum pads using single bumps worked well with the same setting as with the glass substrates. It was necessary to reduce the force in regard to damages of the thinned module, as 80gr/bump results in 17.9kg per DCD chip. An aggressive step down to 20gr/bump resulted in $\approx$ 60% unconnected daisy chain structures and weak mechanical stability. 60gr/bump showed equally good results as 80gr/bump. The double bump approach was tested with the aim to reduce the force even more. Only one of 158 tests (0.6%) failed with a force 22gr/bump and a reduced temperature of 200 °C. Measurements of snake resistances are shown in figure 6.21. The with 2kg slightly coined bumps show a lower and more uniform resistivity than the uncoined assemblies. Figure 6.16 shows a side view of a double bump assembly. The rough cutting edge surface is caused by the laser cutting of the wafer. A cross section of single bump assembly is shown in figure 6.17 with a squashed bump diameter of $105 \mu m$ and a chip distance of $32 \mu m$.

6.5.3 ILC Full Size Demonstrator Module

A large mechanical sample of an ILC module, with a size of $11.9 cm \times 1.6 cm$, was added to the wafer layout in order to test the handling of large devices and the flipping of many chips with low pitches. Landing pads for 36 Switcher3 and 16 DCD2 chips were available on the module, with a total of 9344 bumps. The chips have been flip-chip bonded with the single bump approach, because the module lacks electrical test capabilities and was

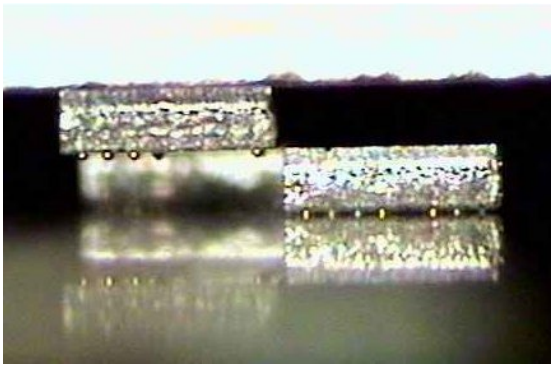

Figure 6.18: Side view of Switcher3 dummy chip being placed with a $50\mu m$ gap to the neighbor chip.

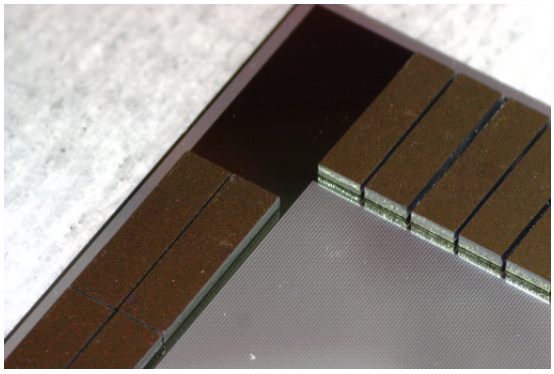

Figure 6.19: Photograph of DCD2 and Switcher3 dummy chips on the ILC mechanical demonstrator module.

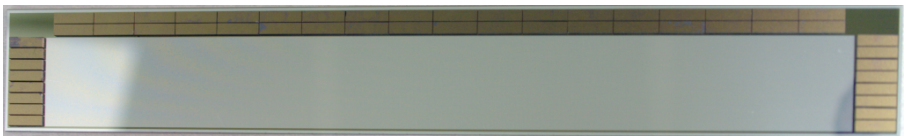

Figure 6.20: Real size photograph of the $11.9cm \times 1.6cm$ large silicon demonstrator assembled with 36 Switcher3 (top) and 16 DCD2 (sides) flip-chips.

only foreseen for mechanical tests. The laser dicing of the dummy chip wafer caused non-flat chip edges due to the misalignment of front- and back side cutting steps. The different chip sizes made a preselection of chips necessary to be able to place the chips accurately. Figure 6.18 displays a side view of the flipping process. A chip is mounted on the bond head and being placed to the substrate. The non-uniform cutting can be seen on its right side.

Flipping the 52 chips with a distance of $50\mu m$ to neighboring chips was doable with the available equipment. Figures 6.19 shows a close-up of the modules corner with Switchers and DCDs. A real size view of the fully assembled module can be seen in figure 6.20. The measured chip sizes have to be taken into account for further module designs, which may differ from the ordered size, especially on multi-project chip productions. Measurements on the DCD2 showed a increased chip size of $26 - 62\mu m$ per edge.

6.5.4 Triple Chip Dummy Substrates

The ILC dummy module is a mechanical sample demonstrating the ability to flip-chip bond with a low chip distance, but it doesn't allow electrical tests. A low pitch device for connectivity testing was necessary. An uncut dummy chip wafer was cut with a different pattern. The substrates were cut in groups of three, while the chips were singularized. Three chips could then be bonded to the substrate sequentially. The large pickup tool

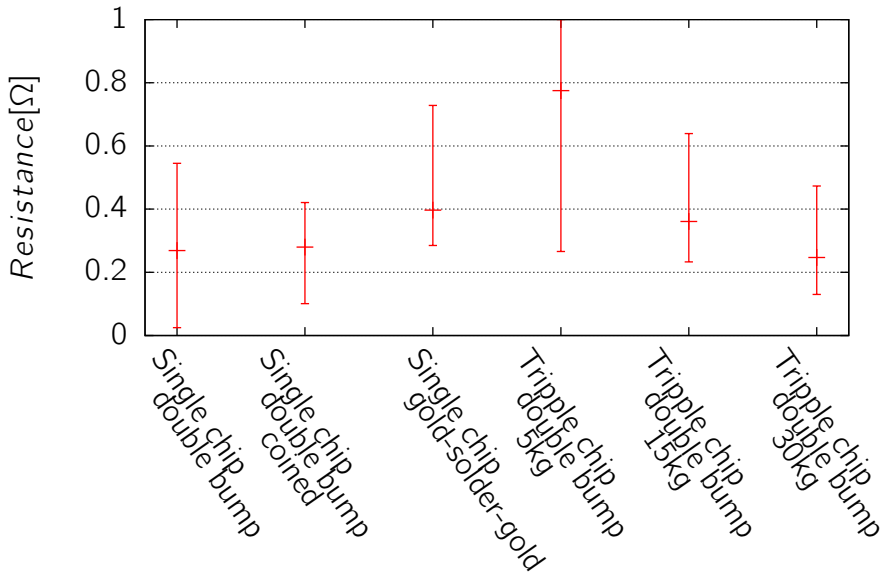

Figure 6.21: Resistances per bump for different flip-chip assembly methods.

covers all three chips and thus, the bonding force had to be increased for each flipping to ensure a force of 22gr/bump for all bumps. Double bumps were used, as they showed better results at the single chip substrate tests.

The triple chip assemblies showed 4.6% chain failures, which had been caused by the much too large pickup tool and the still non uniform force distribution. Repeating the bonding cycle by pressing all chips simultaneously with 45gr/bump didn't reduce the failures significantly. A special tool which fits the chip sizes exactly should be used to apply the force selectively and increase the bonding yield. This has not been tested, as the chip geometries were not yet defined and subject to changes during further circuit developments.

Figure 6.21 shows the resistance for different assembly methods measured by a 4-wire setup. The measured snake resistance is corrected by the trace resistance connecting the pads, but includes the resistance of the aluminum pad itself.

6.5.5 Two Metal Layer Test Chip

In the DEPFET production process, the metal layers are created by sputtering aluminum onto a silicon dioxide insulation layer. This layer is thin and not planarized, causing a rough surface with weak insulation at the trace crossings. The metal layer has also different properties than the test assemblies, because they were manufactured of pre-metallized wafers with a flat metal surface.

A test of the bump bonding impact to the metal and insulation layers of the DEPFET technology was necessary. A bumping test design was included on the DEPFET matrix

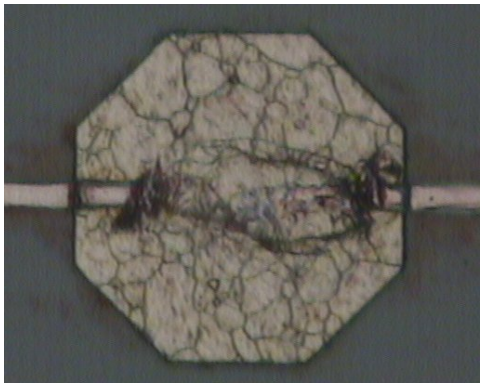

Figure 6.22: Bump pad on wrong layer, trace removed by bump bonding.

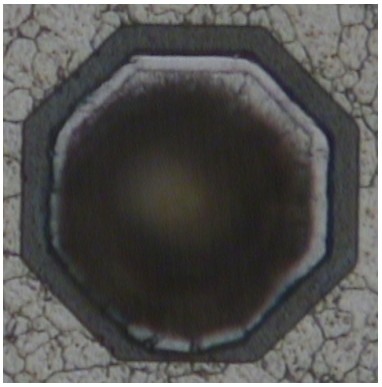

Figure 6.23: Pad metallization pushed outside by gold-stud bump bonding (lower edge).

development run PXD5. Bump pads with different metal layer configurations should give information on the bondability of gold-studs and the impact to the metal layers. A single layer bump pad with traces crossing on the underlying metal was included to test the strength of the insulation layer, which can be broken by the forces during gold-stud bumping and flip-chip bonding.

Unfortunately, bumping on the insulation test structures was not possible, because the data of the first and second layer were accidentally switched during layout transfer. The bump pad was manufactured on the lower layer and covered by the insulation and the test trace. This trace is too small to be bonded on and was removed by the bonding process (figure 6.22). The impact of bonding to the metal is shown in figure 6.23. A bump with $60\mu m$ diameter is placed on an equally sized pad. The slightly uncentered bump causes the pad metal to be pushed away. This can cause shorts to adjacent traces located closer than $4\mu m$ to the pad. The bumps need to be centered and the pads should be at least $10\mu m$ larger than the bump to increase the security margin. This was taken into account in upcoming designs.

6.5.6 Test Structures in a 180nm Technology

In the 180nm technology, commonly used at the Chair of Circuit Design, a bump pad has to be designed with the three uppermost metal layers. The lower layers and the layers defining active devices are in principle available for a circuit design, but they are not used because the bonding forces could cause damages to traces and devices below the pad. A bump pad with $\approx 70\mu m$ diameter is thus blocking much layout area. The circuit has to be designed around the pad, which is increasing the pad pitch or limiting the design complexity.

Test structures have been included on a UMC 180nm chip submission by the chip designer

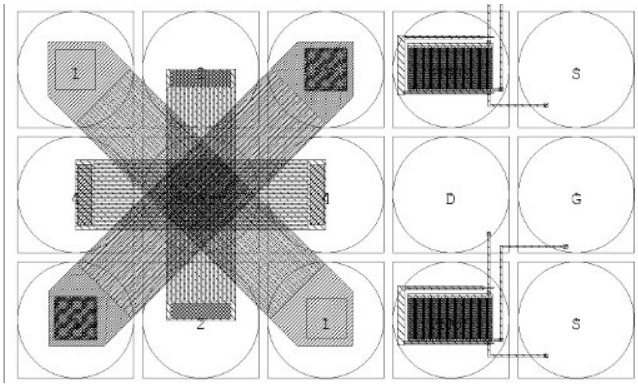

Figure 6.24: Layout of the test structures in UMC 180nm technology.

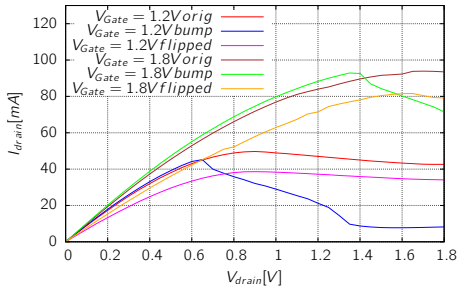

Figure 6.25: NMOS transistor output for different gate voltages before and after bumping and flipping.

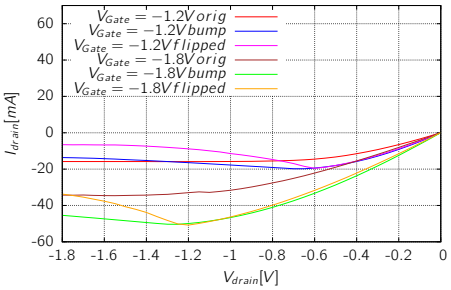

Figure 6.26: PMOS transistor output for different gate voltages before and after bumping and flipping.

to investigate the influence of bonding onto pads above transistors and metal traces. Each chip includes 6 transistors and 4 metal trace tests. Two structures have parallel traces to test for shorts between the layers and two have narrow and long traces to check the connectivity. The three upper metal layers build the bump pad and the three lower, together with the poly-silicon layer, were used for testing. Figure 6.24 shows a part of the test structures with one trace test and two transistors. The bumps are bonded on top of the transistors and to the central pad of the trace test. The adjacent probe pads are connected to the traces and the transistor's terminals.

The structures were characterized before and after gold stud bumping and after applying flip-chip pressure of 60gr/bump with a glass plate. No effects on the metal traces were observed, but the transistors were damaged. Figures 6.25 and 6.26 show the NMOS and PMOS transistors' output characteristics. They are clearly influenced by the bumping and flipping and should not be placed below bump or wire bond pads, while metal traces can be routed below a pad.

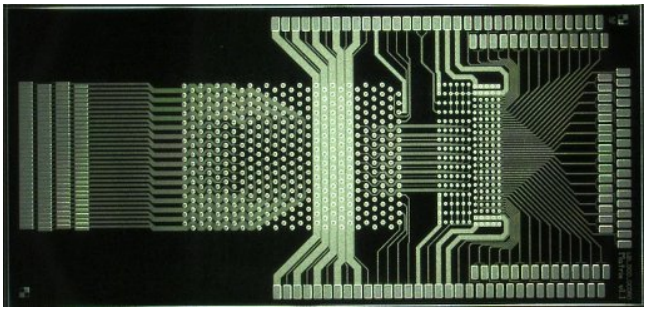

Figure 6.27: Wire bond adapter for DCDB and DCD-RO. Analog wire bond input pads on the left, DCDB in the middle. DCD-RO on the right, surrounded by power and digital I/O pads.

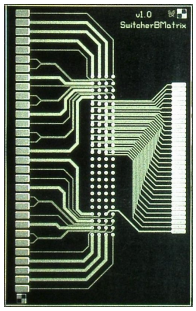

Figure 6.28: Wire bond adapter for Switcher-B. Digital I/O and power pads on the left, gate and clear outputs on the right.

6.6 Wire Bonding Adapters

A set of adapters has been developed during this thesis, which is required to build test systems with the flip-chip only devices DCDB and Switcher-B. They convert the bump-bond footprint to a wire bondable pad pattern, which is compatible to the existing bond pattern of small DEPFET test matrixes and to the pad pitch available in PCB technologies. Pre-metallized 6“ silicon wafers were used and manufactured in an engineering processing chain at the MPI semiconductor lab. The coarser design rules of that processing were sufficient for routing on the wire bond adapters and allowed a faster processing with a reasonable yield. The various adapter designs have been developed and arranged on the wafer area with respect to the dicing ability at an external facility.

The DCDB adapter (figure 6.27) allows to connect all 128 drains of a matrix. The digital output signals are routed to the DCD-RO converter chip, which is located close to the DCDB on the same wire bond adapter. It converts the DCDB's single ended signals to differential pairs, which can be wire bonded to a PCB. Additional sense pads allow measurements of the supply voltages close to the chips, to compensate for voltage drops caused by the sheet resistance of the adapter's aluminum traces.

Two adapter types were designed for the Switcher-B. The first type (figure 6.28) can control a DEPFET Matrix of the PXD6 production (see chapter 7.1). It connects all 16 gate and clear signals of the matrix. The second adapter type is required to operate the matrixes from the previous DEPFET production PXD5, which were designed for the Switcher3. Two chips are needed to provide the gate and clear signals, as the bond pads are located on opposite sides of the matrix. While the gate signals can be connected by the first adapter type, the second type has to be used to connect to the clear pads[1].

[1]The matrix rows would be read out and cleared in opposite directions, if the first type is also used to provide the clear signals. The Switcher-B is rotated by 180° on the second adapter type.

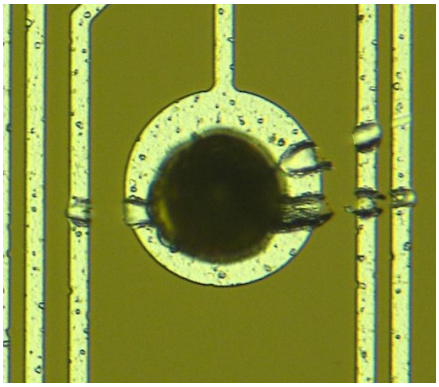

Figure 6.29: Damaged aluminum caused by a touching gold wire due to a bumping machine malfunction.

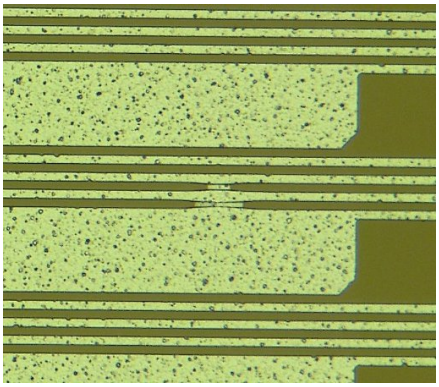

Figure 6.30: Short circuit on a wire bond adapter caused by incomplete etching.

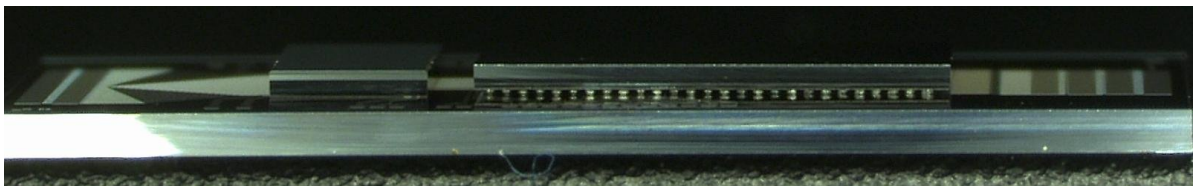

Figure 6.31: Photograph of an assembled wire bond adapter with a DCD-RO (left) and a DCDB (right). The different chip thicknesses are well visible.

The first adapters were produced together with the Belle-type dummy chips and didn't include a passivation layer. They were sensitive to mechanical damages during handling or to machine malfunction during bumping. This caused damaged or shorted metal traces, as displayed in figure 6.29. The next iteration of the adapters included a passivation layer to protect the soft aluminum traces. The adapter close to the wafer edge showed shorts between metal traces caused by dust particle contaminations during lithography or etching (figure 6.30). The adapters were therefore optically inspected and selected prior bumping and flip-chip assembly.

The wire bond adapters were first bumped with gold stud bumps to provide an UBM for the solder bumps of the DCDB and to allow double bump flip-chip for the DCD-RO. In the first step, the DCD-RO was bonded with thermocompression, as it is thinner than the DCDB. The bonding force could not be applied, if the thicker DCDB had been soldered first. The DCDB was then placed on the gold studs and soldered. Figure 6.31 shows a side view of the assembled adapter, with the DCD-RO on the left and the DCDB on the right. The adapter for the Switcher chips were also flip-chip bonded with double bumps.

Positioning errors in the gold stud bumping process caused higher assembly failures. The bump bonder is a flexible machine designed for low volume production or research and development applications with medium pad pitches. It's placement accuracy is limited

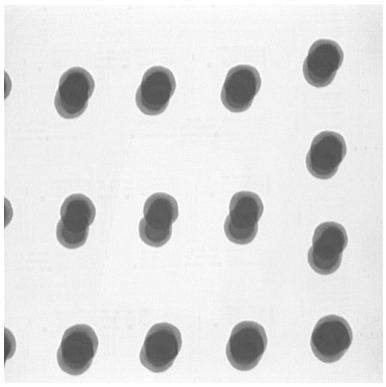

Figure 6.32: X-Ray image of a DCD-RO showing misaligned gold bumps due to positioning errors during bumping. [50]

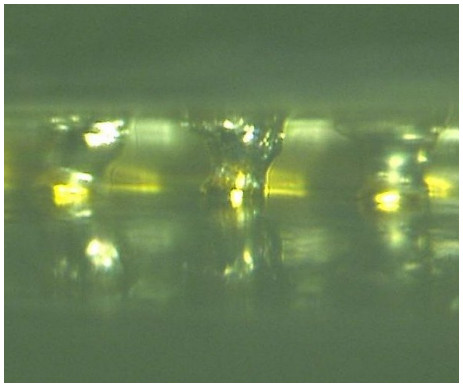

Figure 6.33: Side view of a soldered DCD-RO. The solder is compensating the alignment mismatch.

by the vision system, the software's bond program alignment procedure and the xy-stage control. Many bumps are placed to the pad center, but about every fourth row is $10 - 20\mu m$ off-center. The error was reduced by manipulating undocumented software parameters, but a manual alignment of off-center bumps is still required to achieve a good placement.

Figure 6.32 shows a X-ray image of the DCD-RO with an alignment error of corresponding gold stud bumps of up to $40\mu m$. Solder balls were added to the chip, which compensated the alignment error. The chip has been solder bumped using the jetting technique after coining the gold bumps to provide a flat surface. DCD-RO and DCDB have been placed on the wire bond adapter and a reflow cycle has been started to solder both chips at once. Soldering without flux showed a non-uniform wetting of the bumps. A thin layer of no-clean lead-free compatible flux was applied to the wire bond adapter prior chip placement. A good wetting was then observed. The gold stud mismatch was compensated by the solder, as shown in figure 6.33.

6.7 Contributions to other R&D Projects

Besides working on bonding and flip-chip topics for the ILC and Belle II projects, the knowledge has also been transferred to other R&D groups.

Wire bonding was used to connect test chips to ceramic packages or gold plated printed circuit boards. JLCC carriers were often used for small and low pin count devices (10-68 bonds), whereas higher pin count PGA carriers (100 pins) were used less frequently. Low wire loops are critical when bonding in chip carriers, because a conductive lid can touch wires and cause short circuits or a non-conductive lid can bend wires and cause bond failures or wires touching each other. Bonding to PCBs was often used for various

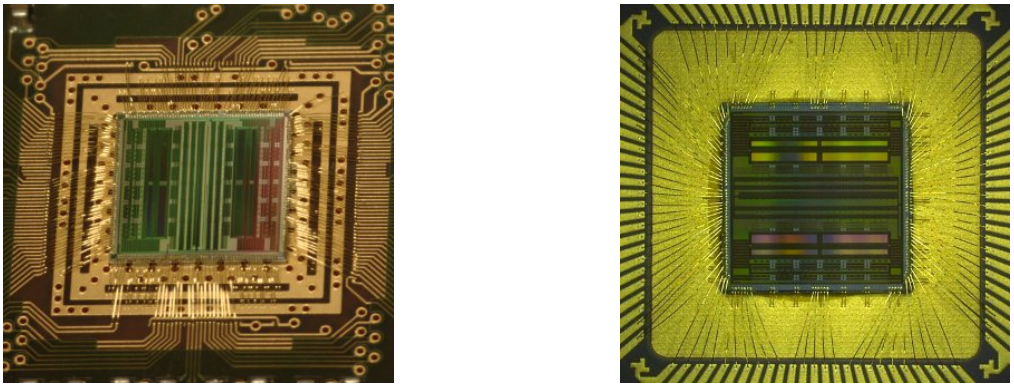

Figure 6.34: Wire bonding of the multi channel read-out ASIC for time-of-flight positron-emission-tomography to a PCB and to a PGA carrier.

devices up to 230 bonds.

Flip-chip was mainly used for interconnecting novel detector concepts with read-out electronics or soldering devices to PCBs. A flip-chip assembly of dies to PCBs is only possible for low pin count devices with a large pad pitch, as the possible pad pitches of the chips are much smaller than the pitches available on PCBs.

6.7.1 HyperImage ToF-PET Readout Chip Wire Bonding

The HyperImage medical imaging project [51] develops a hybrid system of time-of-flight positron emission tomography and magnetic resonance imaging. A multi channel read-out ASIC has been developed, which allows time-stamping in the range of 15 picoseconds [52]. A stack of 3 PCBs contains the silicon photo-multiplier (SiPM) detectors on top, the read-out ASICs in the middle and a controller board at the bottom [53]. Multiple PCB stacks are arranged in a circle and form the detector ring.

Figure 6.34 shows the wire bonding of the timing ASIC to a PCB used in the stack with 230 bond wires and three loop forms connecting power and signal pads. The signal pads on the PCB are only $60\mu m$ wide to allow a low angle wire fan-out. Standard technologies use $100 - 200\mu m$ wide pads. The chip has also been bonded into a PGA chip carrier with 100 pins. Several of the chip's pads had to be bonded to the same destination, with other bond wires in between connecting to the cavity's bottom. The low pin count of the carrier requires to bond with very high angled wires and to bend the wires manually to keep them separated.

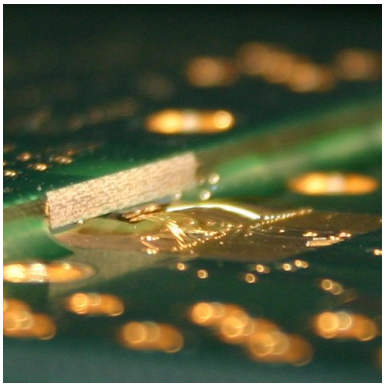

Figure 6.35: Capacitive-Coupled Pixel Detector (CCPD1) placed between two PCB boards and wire bonding of one side.

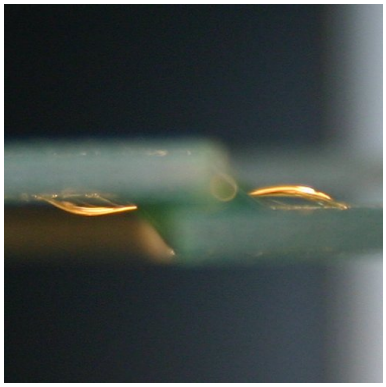

Figure 6.36: Side view of the wire bonding of the detector and read-out chip of the CCPD1.

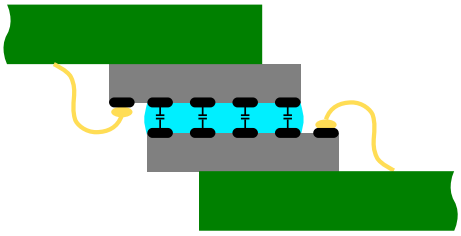

Figure 6.37: CCPD1 Detector assembly principle with PCBs (green) and flip-chip bonded chips (gray) with glue (cyan) to assist capacitive coupling. Both chips are wire bonded.

6.7.2 Capacitive-Coupled Pixel Detector

Monolithic active pixel detectors, integrating detector devices and read-out electronics in the same semiconductor technology, have some drawbacks which can be overcome by hybrid designs. In hybrid pixel detectors, the optimal detector material can be chosen, while the read-out electronics can be designed in a modern deep-submicron technology. Fast read-out electronics and complex circuits fit into the pixel area and perform various tasks like time-stamping, A/D conversion and signal storage. Detector and read-out chips have to be electrically connected using flip-chip bonding for single chips or, on a wafer level, by wafer bonding and 3D interconnect with through-silicon vias. The bump bonding flip-chip interconnection limits the pixel pitch to more than $50\mu m$ for non-standard and expensive technologies and $200\mu m$ for widely available processes [54].

An alternative hybrid pixel detector design has been proposed by I. Perić: Capacitive coupling of the detector signals to the read-out electronics with many small electrodes can reduce the pitch without using low pitch interconnection technologies [55]. Electrodes on the detector and the read out chip are carefully aligned and the chips are flip-chip bonded. Glue is used to fix both devices and to fill the air gap in between the chips.

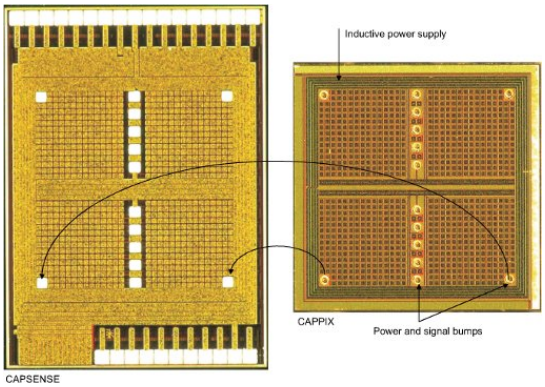

Figure 6.38: Capacitive-Coupled Pixel Detector (CCPD2) and readout chip. [54]

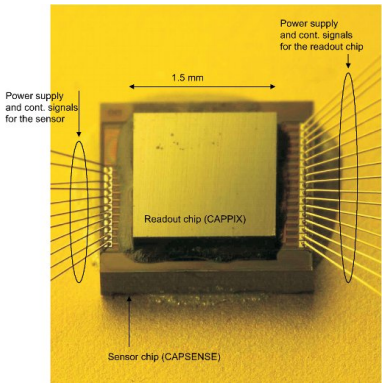

Figure 6.39: Readout chip flipped onto detector with glue and wire bonded in carrier. [54]

The glue also assists the coupling by its permittivity. Bumps bonds can be used to connect power and steering signals. The first design of this novel type included the detector with $78\mu m \times 60\mu m$ pixel sizes, and read-out electronics on the same die, without interconnecting them electrically. The detector and read-out areas of two chips are flip-chip bonded with a non-conductive adhesive to build the hybrid detector assembly. The flip-chip bonding does not provide an electrical connection between the two chips. Choosing the right amount of adhesive to cover all coupling electrodes, but not the wire bond pads at both ends of the assembly, was crucial. The chip assembly was placed in between the two PCB boards and wire bonded. Wire bonding was difficult, as the upper and lower sides of the chip assembly had to be bonded to different sides of the two PCBs (see figure 6.37). Figure 6.35 shows the wire bonding of one side of the flip-chip bonded Capacitive-Coupled Pixel Detector placed in between the two PCB boards. The wire bonding of both sides of the assembly is shown in a side view in figure 6.36.

For the second prototype [56], the detector and the read-out chip were designed in different technologies, allowing smaller pixel sizes of $55\mu m \times 55\mu m$. The read-out chip isn't wire bonded anymore and its power and data signals are connected with bump bonds, while the detector signals are still capacitively coupled (see figure 6.40). The detector is used to route the bump bonded power and signal pads to the wire bond pads at the detector edges. Figure 6.38 shows the two chips with the bump bond pads for power and data transmission and the electrode matrix for the capacitive coupling. A flipped and wire bonded assembly is shown in figure 6.39. The black glue at the edges of the read-out chip increases the permittivity and increases the mechanical stability. The coupling capacitance has been measured to $1.18fF$, which corresponds to an electrode distance of $20\mu m$ for a dielectric constant of the glue of $\varepsilon_r = 3$. An input referred noise of $80e^- RMS$ has been measured.

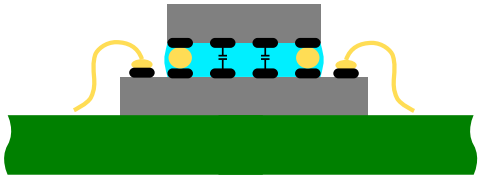

Figure 6.40: CCPD2 Detector assembly principle with the read-out chip (top) flip-chip bonded to the detector (bottom) with glue (cyan) to assist capacitive coupling. Only the detector is wire bonded. Power is supplied to the read-out chip via bump bonds, while the signals are still transmitted capacitively.

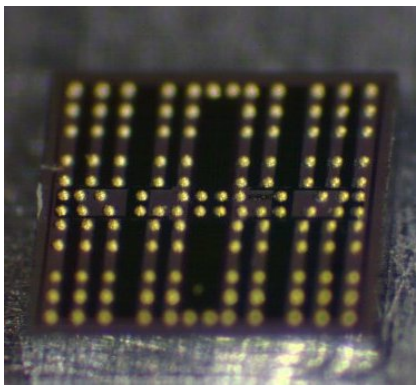

Figure 6.41: Bumped ISOPIX read-out chip.

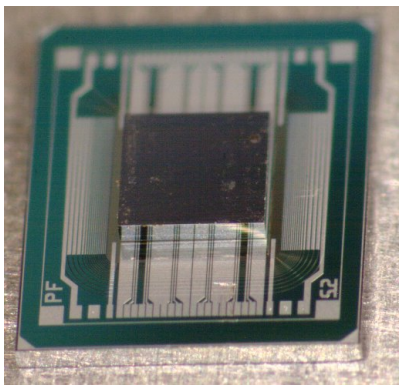

Figure 6.42: ISOPIX chip flipped on ISOSENSOR.

6.7.3 ISOSENSOR & ISOPIX

In normal hybrid flip-chip pixel detectors, the I/O pads and associated electronics in the chip lead to dead areas on the sensor, where pixels cannot be read out. The ISOPIX concept uses a geometry where the I/O bumps are spread *in between* the pixel bumps. In addition, the chip pixels are smaller than the sensor pixels, so that an assembly with many chips without any pixel loss is possible. The chips power and control signals are routed on the sensor silicon.

ISOSENSOR and the ISOPIX chip build a hybrid pixel detector using flip-chip technology to mount the ISOPIX read-out chips on the ISOSENSOR detector substrate. The sensor uses a cheap semiconductor technology, which delivers large area detectors at a reasonable price. A depleted p-doped substrate is used and n-doped regions form the charge collection electrodes. The interconnection can be realized with one metal layer only, which is used to provide the bump pads and traces to connect the power and data lines of the read-out chips. The readout chips are smaller than the detector and multiple chips have to be bonded to large detectors. A pixel size of $150\mu m \times 150\mu m$ and a pitch of $170\mu m$ is used within the read-out chip area, but larger pixels are used to cover the gap in between the chips and to avoid dead areas on the detector. A corner pixel is

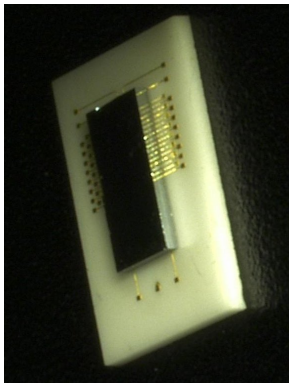

Figure 6.43: XNAP read-out chip flip-chip bonded to ceramic interposer.

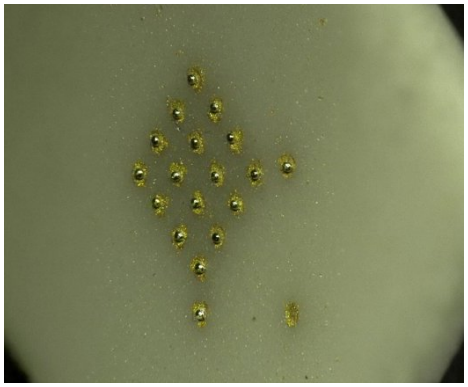

Figure 6.44: Filled through-hole vias in the ceramic interposer with solder bumps.

$225\mu m \times 220\mu m$ large, defining the size of the vertical and horizontal edge pixels to $150\mu m \times 220\mu m$ and $225\mu m \times 150\mu m$. All chips of a column are connected in parallel. Each chip has 2 input pads to set an address. These pads are connected on the sensor to the appropriate supply lines to hard code the chip's address within the column.

The read-out chip is designed in 180nm technology with a size of $1.5 \times 1.5mm^2$ and can read out 100 pixels. A small chip size permits a cheap production and a higher yield. The bump pad diameter is $60\mu m$, which is very small and requires a precise placement of the $\approx 65\mu m$ gold stud bumps. Configuring and read-out of the pixel data are realized with serial shift registers. A chip addressing is used to prevent multiple chips of sending data simultaneously, as all chips within a column are connected in parallel. Figure 6.41 shows the ISOPIX chip with gold stud bumps. The pixel connections are placed in the four corners in groups of 5×5 bumps. The control signals and power supply connections are located in between these groups. The first sensor and read-out chips were wire bonded separately for evaluation and characterization. Figure 6.42 shows a hybrid assembly with a small detector substrate and a single ISOPIX read-out chip [57]. The control and power lines on the detector were routed closely to the bump pads, due to space limitations. An unpassivated detector surface, together with a pad size already smaller than the bump diameter, caused shorts during flip-chip mounting. The bump diameter is increased furthermore by the flip-chip forces and shorted the bump with adjacent traces. Several assemblies showed shorted power and signal traces. It was possible to create a working assembly by reducing the flip-chip force.

6.7.4 XNAP Ceramic Interposer

The XNAP project is developing a X-ray counting detector for synchrotron applications, with a time resolution in the nanosecond range. The detector is based on silicon

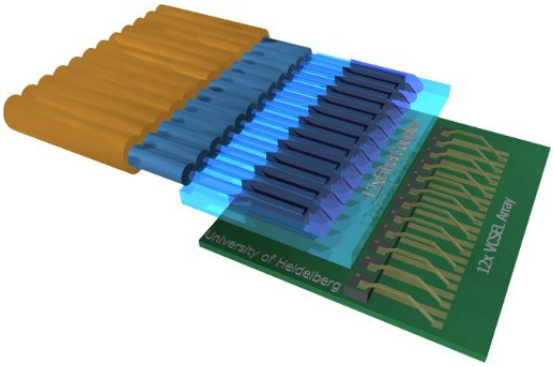

Figure 6.45: Array of 12 fibers with optical coupling and vertical emitting laser array. [58]

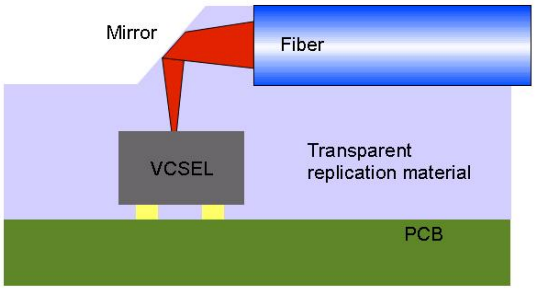

Figure 6.46: Side view of the optical coupling principle. [58]

avalanche photodiodes (APD). The read-out chip supports 16 detector inputs, which are connected to a 4x4 APD detector. A ceramic interposer with filled through hole vias is used to connect the detector with the read-out ASIC and provides a fan-out for the ASIC's power and data signals. The detector is flip-chip bonded to one side of the interposer, while the ASIC is bonded to the other side. Since the detector is pressure sensitive, it cannot be bonded using gold-stud bumps and has to be soldered. The read-out chip had to be mounted first using gold-stud bumps, to allow a soldering of the detector in a second step (figure 6.43). The filling material of the interposer's through hole vias (figure 6.44) was not solderable and caused the detector to fall off. A new interposer based on PCB material was then developed. Gold-stud flip-chip bonding to a PCB is likely to fail, due to the soft PCB material which is not withstanding the required force and temperature. Soldering is a more promising approach. Gold-stud bumps were placed on the chip to provide the under bump metallization for the solder balls. The chip was touching the solder resist of the PCB, because the solder volume of one ball was not enough to provide an appropriate stand-off. The soldering was weak and chips fell off. Placing two solder balls per gold bump provided enough solder volume to create a strong bond and a sufficient gap between the chip and the substrate. The chip were successfully attached to the interposer.

6.7.5 Advanced Optical Cable

High speed networks for short range interconnection in high performance computing are electrically limited to a few meters at 10Gbit/s transmission speed. Optical interconnects based on fibers can enhance the distances. A cheap drop-in replacement for existing electrical interfaces is developed by the High-Speed Short Range Interconnects research group at the Institute of Computer Engineering. An optical conversion of the serial protocol should be integrated into the small casing ($27mm \times 29.9mm \times 6.1mm$) of the

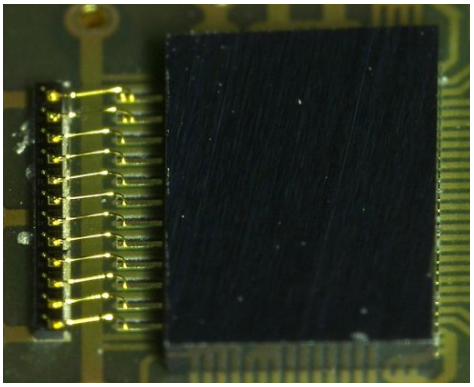

Figure 6.47: VCSEL diode array bonded and driver chip flip-chip soldered to a PCB.

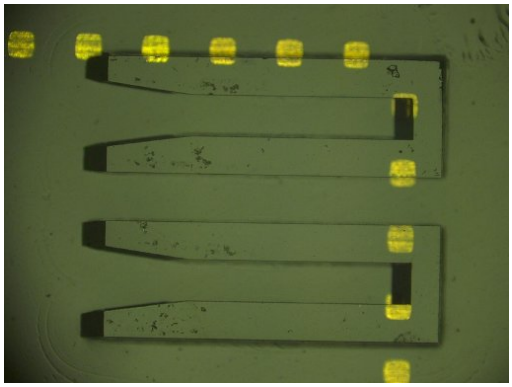

Figure 6.48: Cured adhesive on a test substrate, embossed using the flip-chip equipment

electrical connector, allowing to increase the transmission distance by simply replacing the electrical cable by the advanced optical cable. Fitting the 12 laser- and photo diodes together with the 90° deflection of the optical coupling (figure 6.46) and the 24 fibers into the flat housing is the challenge of this project (figure 6.45). [58]

The laser array based on vertical surface emitting lasers (VCSEL) and its driver chip was mounted on one side of the PCB (figure 6.47). The receiver array and its amplifier are located on the other side and was not yet assembled. A coupling structure is created with an optical adhesive to mount the array of optic fibers parallel to the PCB and couple them to the vertical emitting laser diodes and detectors. It is structured by a preform and cured by ultraviolet light. This adhesive is directly applied to the semiconductor devices and the preform has to be aligned precisely to the semiconductors to maximize light coupling from and to the fibers by the imprinted 45° mirror. Figure 6.48 shows the structure on a test substrate, which was created with the flip-chip bonder. The fibers are places in the notch and are fixed by with glue.

7 DEPFET Module Balcony Design

The DEPFET matrixes of the PXD5 production for characterization of the ILC type designs were tested in setups with the read-out and steering chips wire bonded to the matrix. The novel all-silicon module approach, with flip-chip bonded chips, has not yet been demonstrated with active components.

The first DEPFET matrixes with flip-chip interconnection of the read-out and steering chips were included on the PXD6 wafer run. Different matrix design are used to evaluate the optimal pixel layout for the Belle II vertex detector. Most of the matrixes are still wire bondable for a faster comparison of different matrix types with the same steering and readout chips. They are bonded to PCBs, which can be plugged into the read-out system. Some matrix types have flip-chip footprints on the detector silicon, to build all-silicon modules. Most of the flip-chip matrixes have an active area of 128×16 pixels, which is sufficient for evaluation of the flip-chip module performance. Large matrixes with more than 768×120 pixels are included on the wafer too, to gain information about the production yield and the performance of large matrixes. The wafers will be partially thinned with the technology presented in 3.2. The PXD6 matrixes are the first thinned and bump bondable DEPFET matrixes.

Besides the DEPFET design evaluation, work on the mechanical integration of the modules in the Belle II detector is necessary. A support carrier is needed to mount the modules in two concentric layers around the beam pipe. The data signals and power supply lines have to be routed on a cable through the Belle detector to the DEPFET ladders. The cable has to be securely connected to the modules. Power dissipated by chips and DEPFET transistors has to be removed by cooling and the thermal expansion of the material has to be taken into account for the mechanical designs. The signal routing and cable mounting on the module with a constrained size require training. Two fully populated and thinned half modules have to be glued together to 17cm long and 1.5cm wide ladders with up to 50cm long cables at both ends. The assembled modules have to be mounted on the support structure with less than $100\mu m$ clearance to adjacent components. This challenging approach has to be tested. It was decided to build the modules without the active DEPFET pixels to save production time and manufacture only the metal layers needed to test the electrical behavior of the steering and read-out chips. The design should be as close as possible to a final layout. This electrical multi chip module (E-MCM) will contain 4 DCDs together with 4 DHPs and 6 Switchers.

During this thesis, the bump bond layouts of the PXD6 matrix balconies and the layout of the E-MCM were created.

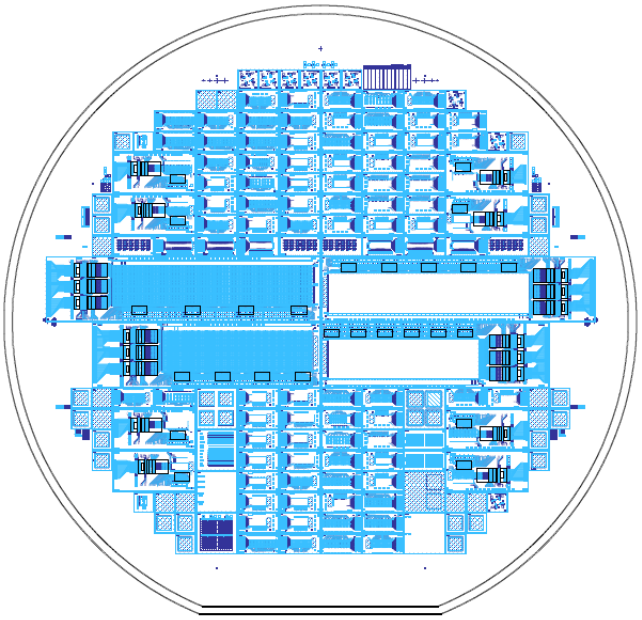

Figure 7.1: 6“ wafer of the PXD6 DEPFET production to evaluate design options for the Belle II detector. 87 wire bond and 8 bump bond matrixes with 128×16 pixels and 4 large bump bond matrixes with up to 768×180 pixels are contained.

7.1 PXD6 Matrix Designs

The PXD6 matrix development wafer run is used to evaluate DEPFET design options for the Belle II detector modules. Pixel lengths between 50 and $200\mu m$, the clear gate capacitively coupled to the clear signal or enhanced drift regions, realized by different implantation profiles, can be compared. As the DEPFET production is an engineering process, new wafers might show different properties than previous productions. A technology comparison is possible with unmodified ILC-type designs from the PXD5 run which were included on the PXD6 wafers. Figure 7.1 shows the 6” wafer with four large matrixes in the middle and small matrixes and test structures above and below.

Most designs are small matrixes ($0.5 \times 1cm^2$) with 128×16 pixels, which have to be wire bonded to wire bond adapters with the steering and read-out chips mounted (figure 7.2). Bonding the matrixes to interchangeable PCBs allows to compare designs with the same steering and read-out chips. A few of these small 128×16 matrixes have flip-chip layouts with read-out and steering chips mounted directly onto the detector silicon (figure 7.3). One DCDB and one Switcher-B is needed for a small module of $1cm$ width and $2cm$ length. This allows an evaluation of matrix and chip behavior with the all-silicon approach.

Additionally, four large matrixes with 768 drains and between 120 and 180 rows were designed (figure 7.4). The number of rows depends on the selected pixel length and

results in $1.5cm$ wide and $5.5cm$ or $6.5cm$ long modules. 3 DCDBs and up to 6 SwitcherBs are mounted on a large matrix. These large matrixes should give a yield estimation of the DEPFET pixels and show the DCDB's performance with the high capacitive load of the long drain lines. Long matrixes have not been operated yet with multiple Switchers or DCDBs. Knowledge on synchronization of multiple read-out and steering chips is gained and the all-silicon module concept is demonstrated.

The size of the modules and the active area was designed by the MPI Semiconductor Lab in Munich. The signal routing of the steering and read-out chips was designed as part of this thesis. The DHP footprint was not included in the first PXD6 bump bond designs, as it was not ready during the design phase and the DCD-RO was used instead. It was decided to manufacture most wafers with the DCD-RO based read-out, as it was successfully tested on the wire bond adapters. The DHP replaced the DCD-RO in an additional wafer design, which was manufactured in the second production batch. The PXD6 design changes were made by the DHP developers at the SiLab of Bonn University. Two PXD6 wafers were manufactured with the DHP footprint, while the others are based on the DCD-RO. 87 small matrixes with 36 different designs are included on a wafer. Four small matrixes feature the bump bond option and four matrixes are of the large type.

7.1.1 Technology Properties

The PXD6 production provides two poly-silicon layers for the DEPFET gate and clear-gate structures. Two aluminum metal layers with a sheet resistance of $30m\Omega/\square$ are available for routing the power supplies and the data signals. Gold stud bumps have to be used to interconnect the flip-chip devices, as the pad metallization is aluminum and an additional under bump metallization is not available.

Since the test structures presented in chapter 6.5.5 couldn't provide information on the insulator stability and the impact of bumping on pads with traces routed below, this routing option was avoided. The traces are routed in between the bumps with at least $7\mu m$ distance to pads, to accommodate the pad deformation during uncentered bump placement. A bump pad is designed with both metal layers, as this design showed a good bondability on the bumping test structures. Poly-silicon is forming a barrier layer below each bump pad and thereby prohibits shorts between the bulk material and the metal layers.

The insulation layers are not planarized and cause a rough surface, in contrast to commercial processes with utilize chemical mechanical polishing (CMP). Parasitic capacities of planarized technologies can be extracted with the standard tools included in the design software packages. Non-planarized layer build-ups, as in the DEPFET technology, can not be approximated by these tools, due to the more complex electrical field. Special tools have to be used, which are aware of the special geometry and can estimate the

capacitive properties. These tools were not available during the design phase and the capacitive load on the signal traces had to be approximated. The capacitance of the parallel-plate capacitor can be calculated with equation 7.1. Besides the plate capacitance, the fringe capacitance (approximated by equation 7.2 [59]) and the capacitance to adjacent metallization lines (approximation by equation 7.3 [60]) have been taken into account.

$$C_{area} = \varepsilon_0 \varepsilon_{SiO_2} \frac{wl}{t_{ox}} \tag{7.1}$$

$$C_{fringe} = \varepsilon_0 \varepsilon_{SiO_2} \left(1.06 \left(\frac{w}{t_{ox}} \right)^{\frac{1}{4}} + 0.77 + 1.06 \sqrt{\frac{t}{t_{ox}}} \right) \cdot l \tag{7.2}$$

$$C_{neighbour} = \varepsilon_0 \varepsilon_{SiO_2} \left(1.15 \frac{w}{t_{ox}} + 2.8 \left(\frac{t}{t_{ox}} \right)^{0.222} + B \right) \cdot l \tag{7.3}$$

with

$$B = \frac{0.06 \frac{w}{t_{ox}} + 1.66 \frac{t}{t_{ox}} - 0.14 \left(\frac{t}{t_{ox}} \right)^{0.222}}{\left(\frac{w_{gap}}{t_{ox}} \right)^{1.34}}$$

The active area will be thinned to $50\mu m$. The balcony and end-of-stave areas won't be thinned, as gold-stud bumps and wire bonds have to be bonded and possibly cause damaged to the thin material. It has a thickness of $450\mu m$. A passivation layer is added to protect the metal layers from damages. The active area is not covered with passivation, as the sensor engineers are concerned that mechanical stress that might break or deteriorate the thin DEPFET transistors. The next section shortly presents some details on the various designs.

7.1.2 Wire Bond Matrixes

A fan-out was designed for the wire bond matrixes. It connects the gate and clear lines of the active area to wire bond pads located at the side of the matrix. The development of the wire bond adapters and the matrix fan-outs had to be synchronized. The single routing layer of the adapters limits the signal re-ordering capabilities and therefore the pin-out of the wire bond pads is defined by the adapter routing. A re-ordering had to take place on the matrixes, as there were two metal layers available. It was only necessary for the ILC-type matrix designs.

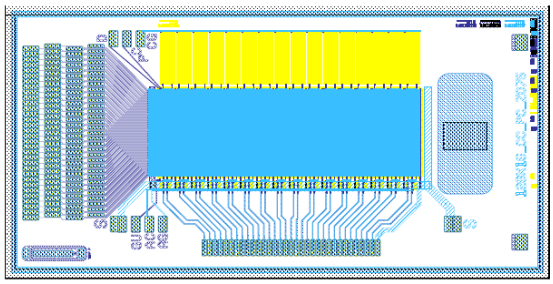

Figure 7.2: 128×16 pixel DEPFET matrix of PXD6 production with wire bond pads.

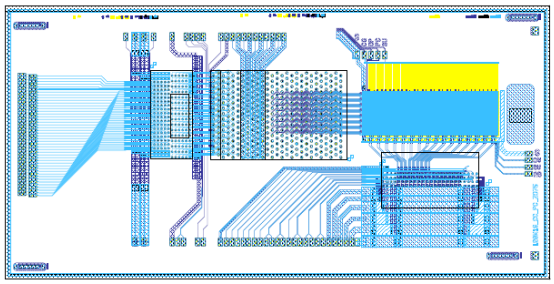

Figure 7.3: 128×16 pixel DEPFET matrix of PXD6 production with bump bond footprints for DCDB, DCD-RO and Switcher-B.

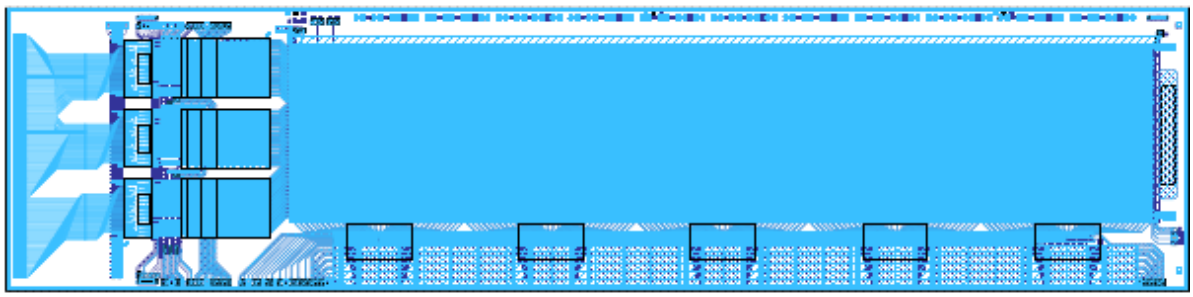

Figure 7.4: 768×160 pixel DEPFET matrix type 768x160_ST_SD_SCG_z075 of PXD6 production with bump bond footprints for DCDB, DCD-RO and Switcher-B.

Figure 7.2 shows a wire bond matrix. The active area with 128×16 pixels is located in the middle. The routing of the 16 clear and 16 gate signals is located below the active area and the wire bond pads of 128 drain lines are on the left.

7.1.3 Bump Bond Matrixes

The bump bond matrixes include footprints to flip-chip mount DCDBs with DCD-ROs and the Switcher-Bs on the detector silicon. All power, control and data signals to the chips and the bias voltages for the matrix have to be connected by wire bonds.

At first, the large bump bond matrixes were developed, to reuse design parts on the smaller matrixes. Figure 7.4 shows the $1.58 \times 6.6 cm^2$ large module with 768 drains, 160 Switcher-B channels, standard clear-gate biasing, standard implantation profiles for the drift regions, a clear-gate surrounding the transistor and a row pitch of $75 \mu m$. The proposed 4-fold read-out for the Belle II detector has been realized and results in a matrix with 192×640 pixel. 3 DCDBs and DCD-ROs digitize the 768 drain currents and 5

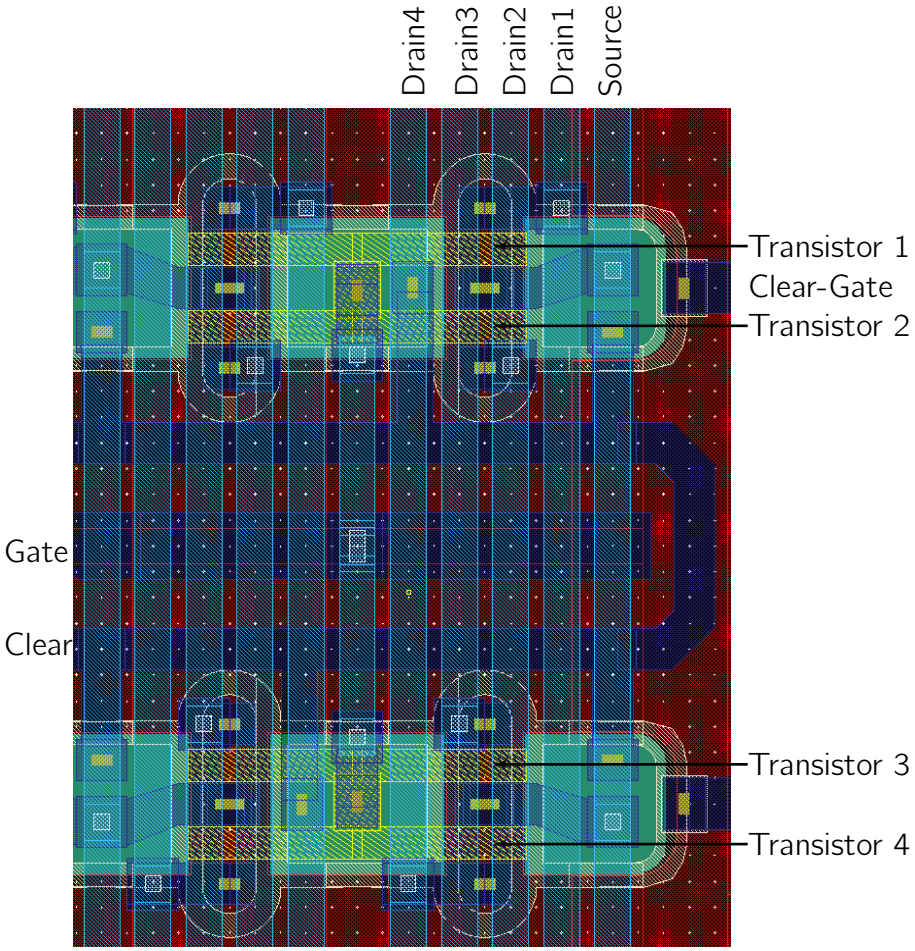

Figure 7.5: Layout of 8 DEPFET transistors with 4-fold read-out. The shown area covers roughly 2x4 pixels which are read out by one gate/clear row and 8 drain lines.

Switcher-Bs provide the 160 steering channels.

The routing on the bump bond matrixes is complicated and thus a means of checking for a correct interconnection of the chips and the matrix is mandatory. A layout-versus-schematic (LVS) check is commonly used to fulfill this task. It extracts devices like transistors, resistors and capacitors defined by geometrical rules from the shapes on the different layers in the layout. These devices are interconnected by the metal traces and vias to generate a netlist. This layout netlist is compared to the schematic and differences are marked as errors. The LVS configuration files defining the devices, metal and via layers are normally provided by the semiconductor foundry, but LVS was not yet used in the DEPFET process and thus the files were not available. The LVS check for the PXD6 DEPFET technology was set up and allows a blackbox LVS, where devices are not extracted but interconnection checks are still possible. The building blocks of DCD and Switcher footprint, matrix frame and wire bond pads are defined as blackboxes and their interconnection is compared to the schematic.

To illustrate the 4-fold read-out, 8 DEPFET transistors are displayed in figure 7.5, with 4 transistors being labeled. The vertical, light blue lines are the drain and source bus lines running on the top metal layer across the full length of $4.8cm$ of the active area. They are connected to the p^+ implantations of the transistor via the lower, dark blue metal layer. Horizontal traces distribute the clear and gate signals of the Switcher-B chip. The DEPFET transistor's external gates are designed with the 2^{nd} poly-silicon layer (yellow). Two groups of four transistor are shown, which are all connected to the same gate line in the middle. The clear areas are colored green, denoting a n^+ implantation. An external clear-gate bias voltage is connected to the 1^{st} poly-silicon layer (gray) surrounding the DEPFET transistor and the clear regions.

Switcher Balcony on the PXD6 Bump Bond Matrix

A $3600\mu m$ wide balcony is available for routing and placing the Switcher chips and signals. The chips have been placed as closely as possible to the active area (figure 7.6). Between the chip bumps and the matrix are $800\mu m$ available for the fan-out of the DEPFET steering signals. The traces are $14\mu m$ wide and have a distance of $4\mu m$ to adjacent metal. The relatively large gap has been chosen as a precaution measure to avoid shorts, although a smaller gap would be manageable. The longest line of a fan-out is $7.7mm$ long[1]. A single metal layer line of this length would have a resistivity of $\approx 16.4\Omega$. It can be reduced by a factor of 1.8 to $\approx 9\Omega$ by using both metal layers in parallel, wherever possible. Both layers can be used on a length of $6.9cm$ of the $7.7cm$ long trace. A estimation of the line capacitance, together with the expected matrix capacitance of $50pF$, leads to a full swing signal rise time of only $530ps$.

The vertical power supply traces are located on the opposite side of the Switcher's bumps.

[1]Matrix type ARR_768x120_CC_ED_SCG_Z100 with $100\mu m$ pixel pitch

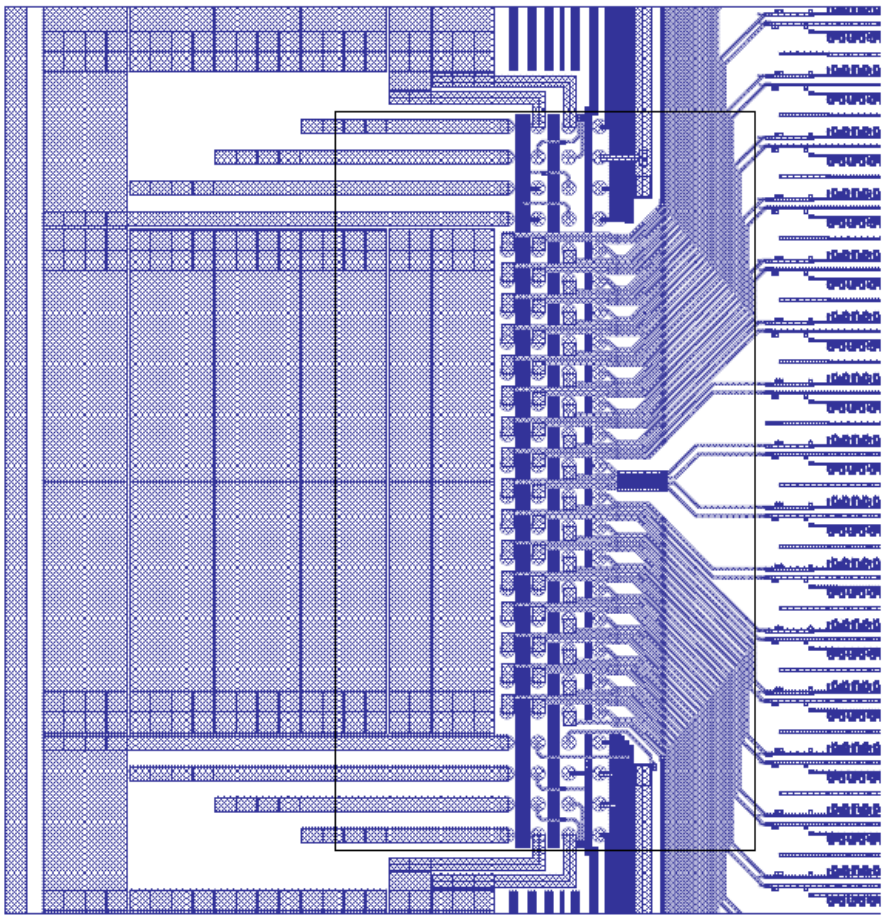

Figure 7.6: Switcher-B balcony layout showing one metal layer. Power buses use both layers where possible to reduce voltage drops.

Four equally wide buses supply the gate and clear on and off voltages. Two additional traces are needed for the Switcher's digital supply. They share the 2300μm wide space, using 410μm for each steering voltage and 500μm for both traces of the digital supply. Continuous top layer metal traces are used to distribute the voltages along the balcony. The chips are connected to the supply lines with horizontal traces on the lower metal layer. The lower metal layer is used in between these connections to double the top layer traces (see figure 7.6). A single line trace resistance of $\approx 3.14\Omega$ can be reduced by a factor of 1.7 to $\approx 1.85\Omega$ by the doubled traces. The voltage drop at the balcony's end is 49mV, with an expected current consumption of 25.6mA on the gate and clear voltages. Additional wire bond pads at the balcony's end are foreseen to measure the voltage drop or to supply the voltages from both ends, in case of a problem.

The steering signals are routed in the space between the power buses and the fan-out. All except of two data signals from the JTAG interface and the channel shift register are distributed to all Switcher chips on long buses. The space is limited at the Switcher's footprint and the traces have to be routed between the bumps or to the right of the chips. A maximum trace width of 14μm could be used in the footprint area. The width can be increased to 30μm between two chips, to reduce the resistivity, but this also increases the capacitance. The lumped C calculation method has been used to estimate the benefit of wider traces. The fastest rise time of 3.2ns could be achieved with 14μm wide double layer traces.

End of Stave

The read-out electronic is located at the end of stave (figure 7.7). Three fully connected DCDBs digitize the active area's drain currents. The matrix drain signals are routed on both metal layers from the end of the active area to the DCDB's input bumps. The DCDB data outputs and steering signals are connected to the closely located DCD-RO converter chips. The 270 differential signals of the DCD-RO are routed to the wire bond pads at the end of the module.

The DCDBs power supply bump layout is optimized for routing on the module. Five horizontal bump rows provide five supply voltages to the chip. Horizontal power buses can be routed across all DCDBs, connecting the chips in parallel. Supply currents of up to 575mA per chip and voltage cause a large voltage drop on the metal traces. If three chips are connected in parallel, the voltage drop at the middle chip would increase to 0.47V, even when both metal layer are used and the traces are wire bonded at both ends. It can be reduced to $< 138mV$, if every chip is supplied separately. The voltages at the chips are monitored with sense lines, to compensate the voltage drop on the traces between wire bond and bump pads. This approach increases the number of power supplies by the factor of 3, as every voltage of each chip has to be regulated. An additional copper layer will be used in the final design to avoid separate supplies. In chapter 7.2 is a layout presented, which utilizes the copper layer.

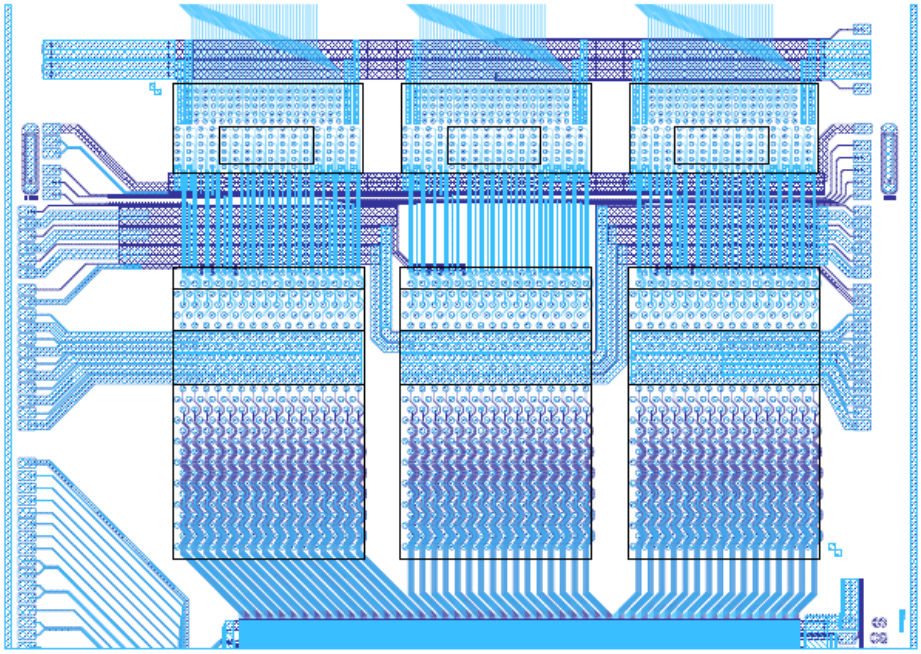

Figure 7.7: End of Stave with 3 DCDBs and 3 DCD-RO. Each DCDB's power is routed separately.

Small Bump Bond Matrixes

Figure 7.3 showed a 128×16 pixel matrix with bump bond pads. The Switcher is shown at the bottom with the fan-out connecting the steering signals to the active area above. The wire bond pads of the control and power signals are located left of the chip. The 128 drain lines of the matrix are connected to one DCDB. The same DCDB input channels were used as on the wire bond adapters, to be compatible with the readout software. The balcony and the end of stave layouts have been copied from the large matrixes and were slightly adjusted. Placing the pads at nearly the same position on the different module types allows the use of the same PCB layout for all small bump bond matrixes.

7.1.4 PXD6 Production

10 wafers are processed and split into two batches after implantation and deposition of the poly-silicon layers. This precaution is needed to accommodate the risk of a weak insulation at metal trace crossings. The first batch with 4 wafers includes designs with DCD-RO only. Tests showed a yield of 80% of small matrixes. Nevertheless, most of the defective matrixes can be used for evaluation, since only some drain lines or matrix rows are damaged. The problems might be caused by lithography, insufficient metal etching or shorts in dielectrics [61].

The second batch includes some patches to work around the problems of the first batch.

Figure 7.8: Photograph of the back side of the first $50\mu m$ thin PXD6 wafer. The cavities where the silicon is etched back are clearly visible. [63]

Two of the six wafers are manufactured with the modified routing design, replacing the DCD-RO with the DHP. These wafers will be processed with an additional copper layer to form an under bump metallization for soldering. [62]

Figure 7.8 presents the back side of the first thinned DEPFET matrixes produced at MPI Semiconductor Lab in Munich. The four big bump bond matrixes are located in the middle, while the smaller matrixes are at the left and the right edges.

7.1.5 First Measurement Results

The first measurements of a thinned PXD6 matrix were made with the well known ILC read-out system at low speed. A 450μ thick matrix of the Belle II design showed a S/N of ≈ 29. The $50\mu m$ thin device of the same type has a very similar S/N of ≈ 31.

A thin PXD6 matrix has also been connected to the Belle read-out system. Figure 7.9 presents a 32×64 pixel matrix with a pixel size of $50 \times 50\mu m^2$. It is bonded to the DCDB read-out chain and controlled by a single Switcher-B. The second Switcher assembly shown is not connected to the matrix.

The matrix could be read out at the maximum DCDB speed of $320MHz$, resulting in the anticipated row read-out speed of $100ns$. The achieved S/N of 17 is not yet optimal, because the DEPFET has to be operated with reduced bias settings. Optimal settings would cause a drain current of $\approx 100\mu A$, while the DCDB's current subtraction cell is

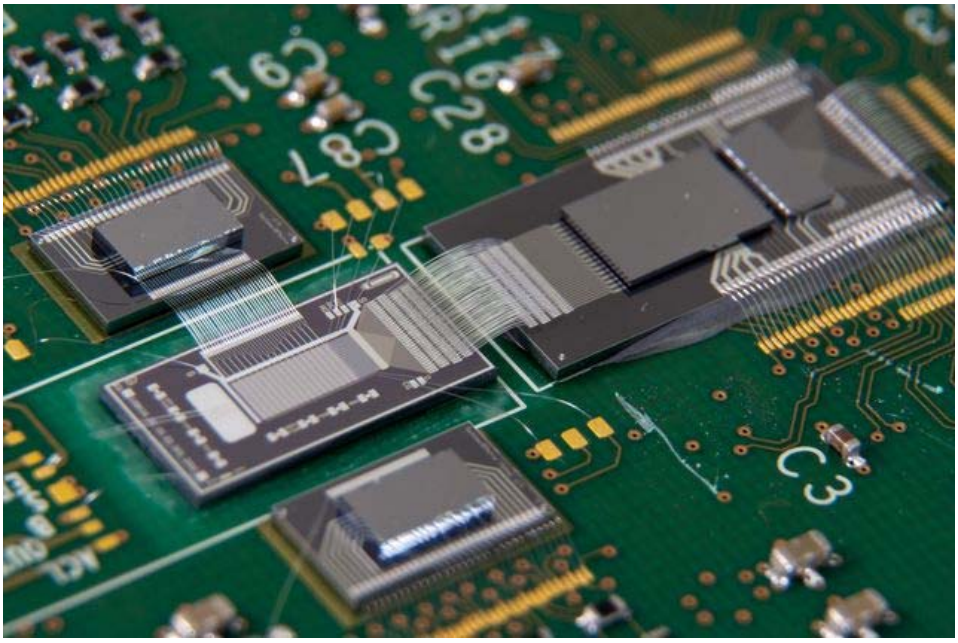

Figure 7.9: Photograph of PXD6 matrix mounted on hybrid PCB and bonded to DCDB and Switcher-B wire bond adapters. The second Switcher-B, used for PXD5 matrixes, is not bonded to the matrix. [64]

only capable of sinking $70\mu A$. The lower drain current results in a smaller g_q, which is limiting the signal to noise ratio [64]. A milestone has been achieved by reading out a thin DEPFET matrix with the Belle II steering and read-out chain including the bump bond chip interconnection.

7.2 Multi Chip Module

The Multi Chip Module is a full size module close to a final design for the Belle II detector. It includes all components required to build an all-silicon module, except the active DEPFET devices, because they would increase the production time significantly. The MCM will be used for system tests like power supply routing, signal integrity, cooling, production yield, kapton cable connection, flip-chip mounting and ladder assembly.

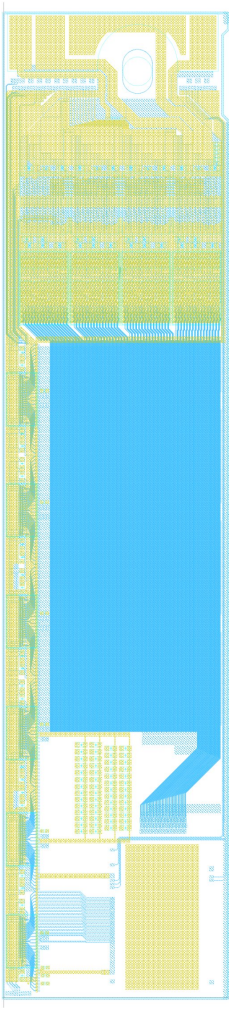

Figure 7.10: $1.5 \times 6.8 cm^2$ large Multi Chip Module.

The first thinned DEPFET modules have been developed with the PXD6 DEPFET prototype production. They allow the characterization of long matrixes with the steering and read-out chips mounted on the detector silicon, to test the all-silicon approach. But still, they don't reflect the geometries and technological properties of a pixel detector module for the Belle II experiment. The layout of all mechanical and electrical components has to be exercised and the systems have to be assembled to reveal yet unknown problems. Processing a DEPFET production needs many months and thus it was decided not to include active DEPFET devices on the Multi Chip Module (MCM). Processing of the metal layers only is faster and still allows to operate the steering and read-out chips.

An inner layer half module's active area is $44.8mm$ long and $12.5mm$ wide, compared to the $48 \times 9mm^2$ of a PXD6 matrix. The dimensions of the module itself is $68 \times 15.4mm^2$, compared to the $66 \times 15.8mm^2$ of the PXD6 module. A wider active area together with the narrower module reduces the available space on the Switcher balcony. The signal and power supply routing has to be adjusted to these changes.

More space is available on the end of stave, but the 4-fold read-out with 1000 drain lines demands four pairs of DCD-B/DHP read-out chips. The routing of data and control lines, together with many supply lines providing the high power requirement of the chips, is a challenge. On the PXD6 modules, the power supply and control signals are routed to wire bond pads to be connected to a PCB. Each DCD-B was supplied independently. This connection scheme is not available for the pixel detector, due to space and material budget limitations. The power supplies have to be combined and all power, control and data signals have to be aggregated at one point at the end of the module. There they are connected to a thin kapton cable.

The mechanical boundary conditions limit the size of the module, as they have to be placed in two concentric layers around and as close as possible to the beam pipe. The modules are mounted on a support structure, which also provides cooling. It contains channels for CO_2 coolant and nozzles to blow dry air in between the layers. The silicon modules are fixed to the cooling blocks by screws, their positions have to be agreed upon by the different designers of the cooling block, the kapton cable and the module layout. The low radii of the layers cause a minimum distance between the overlapping modules. The wire bonds connecting the kapton to the silicon would be destroyed be the overlapping module. A cut-out was introduced to create space for the wire bond looping.

An increased module layout complexity and high power consumption demands for an additional metal layer in the semiconductor technology of the DEPFET sensors. The PXD6 was designed with two metal layers only and required many supply and sense lines to provide the power to the DCDBs with an acceptable voltage drop. The additional metal layer is based on copper and provides by a factor of 6 lower resistivity, but it has not yet been added to a 2-layer DEPFET production. Yield problems on the 2-layered PXD6 wafers' metal structures can be addressed and evaluated on the MCM design, especially in conjunction with the 3rd metal layer.

Two different MCM designs are manufactured: One includes the metal layers of a DEPFET matrix in the active area to measure the parasitic capacitances and to check the yield issue (see figure 7.10). The other layout has test structures in this area, needed to operate and to test the chip performance.

7.2.1 Switcher Balcony

The Switcher balcony layout of the MCM is comparable to the PXD6 layout. Figure 7.11 shows a single Switcher with routing and decoupling.

The first layer is used to route the control and strobe signals, as well as the JTAG slow control from the DHP chips to the Switchers. The digital power supply located left of the bumps is also routed in long buses to all chips. The second layer interconnects the chips with the buses and with the gate and clear lines of the matrix area.

Termination resistors for the differential signals are not yet included into the chip and discrete surface mount resistors with a size of 01005 ($0.4 \times 0.2mm^2$) had to be added to the MCM layout. Wire bond pads are foreseen to short circuit the serial input and output lines in case of a broken Switcher. The resistor and the wire bond jumper pads are located in the 'active area' and are only needed for the MCM design. The final Switcher production will include the termination resistors.

The right picture in figure 7.11 shows the 3rd metal layer. It is used to provide the bump landing pads in the solderable copper metallization. Due to its low resistivity it is also used to route the matrix steering voltages: Narrow lines are used for the less critical clear and the gate-off voltage. The gate-on lines are twice as wide, as these voltages

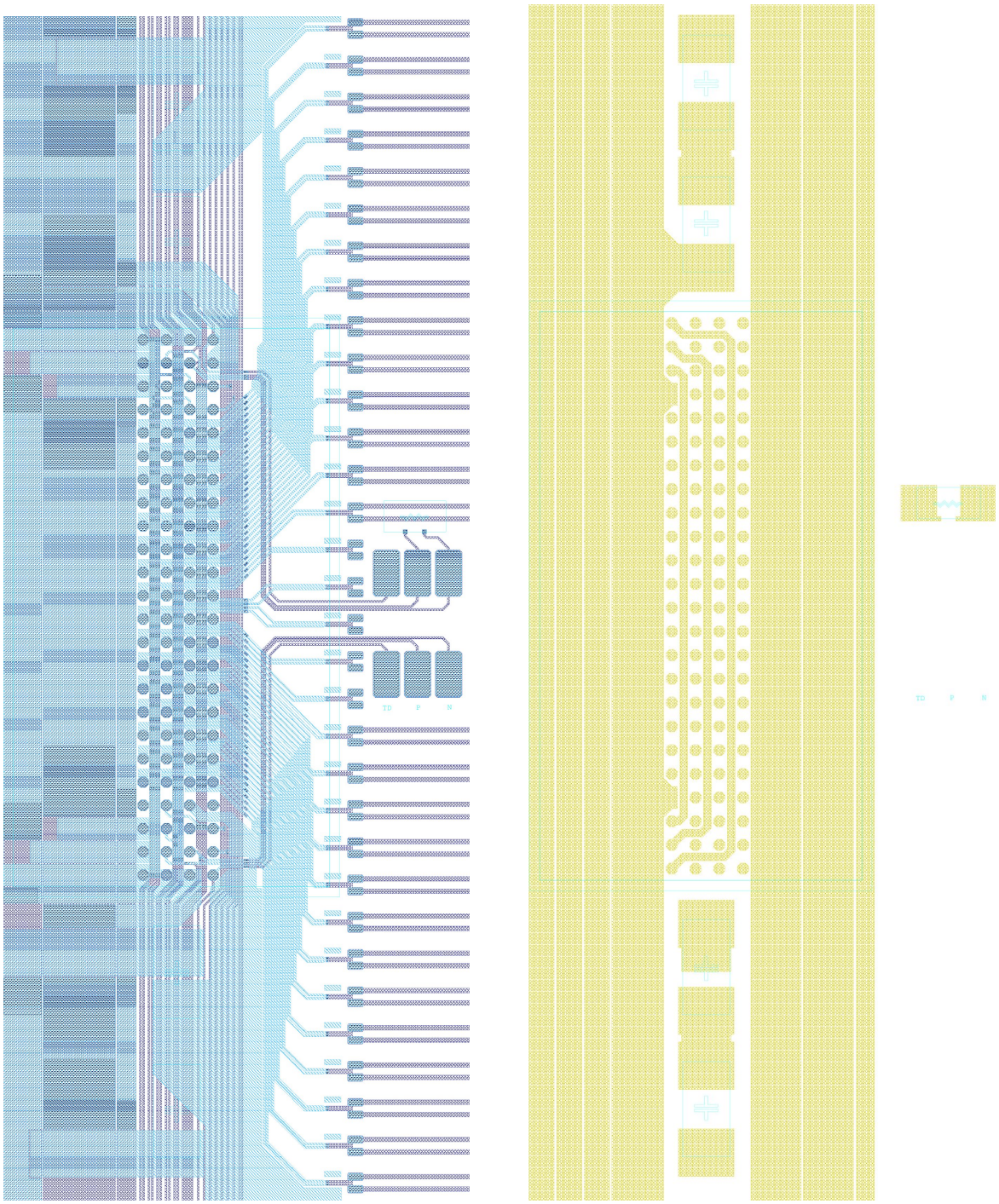

Figure 7.11: Routing on the Switcher balcony for one chip with the first two metal layers in the left and the 3rd metal layer on the right picture.

Supply name	Voltage at cap.	Number of capacitors	Capacitance per cap.	Total capacitance
VDD	3.3V	3	220nF	660nF
VDD_{JTAG}	1.8V	2	220nF	440nF
per Gate On	10V	3	10nF	30nF
Gate Off	-3 .. 5V	3	100nF	300nF
Clear On	17V	3	1nF	3nF
Clear Off	5V	3	100nF	300nF

Table 7.1: MCM Switcher balcony decoupling capacitor numbers and values for a inner layer module.

influence the DEPFET drain current directly. A nonuniform background radiation of the SuperKEKB accelerator may cause different transistor threshold voltage shifts along the matrix length. Three gate-on voltages are therefore foreseen to segment the matrix and to compensate for the shifts appropriately.

Power supply and decoupling

In particle detectors, the power supplies are located far away from the current consumer. A voltage drop is induced by the resistivity of the supply cables. Sense lines are therefore foreseen to compensate for this and to ensure correct voltages on the module. In case of the Switcher, the sense lines are connected to the power buses at the beginning of the balcony. The main voltage drop is caused by the cable while the voltage drop on the balcony is small (see table 7.2). Each digital supply and ground, as well as the gate and clear voltages can be sensed. Sensing can compensate low frequency voltage changes due to the inductance of the long supply cables. Transient events caused by switching digital logic or the matrix control lines with $12.5MHz$ need decoupling capacitors close to the load. Discrete capacitors with a size of 0201 ($0.85 \times 0.35mm^2$ layout area) are placed at both Switcher ends (see right picture in figure 7.11). This size has been chosen as it offers 25V capacitors needed for the matrix steering voltages and fits well into the gap in between the power buses. With the X5R dielectric are decoupling capacitors with $1nF@25V$, $2.2nF@16V$, $10nF@10V$, $100nF@6.3V$ and $220nF@4V$ available [65]. An optimal capacitor value can be chosen for each voltage.

The critical gate-on voltage of nominally 6V relative to Vsource can be decoupled with 10nF per capacitor, if a radiation induced voltage shift of 3V (see chapter 3.4.5) is taken into account. Four capacitors can be placed in between the Switchers at the $60\mu m$ pitch matrix rows, while at the last Switcher in the $55\mu m$ region two capacitors have to be omitted. Table 7.1 lists the number and values of the decoupling capacitors on the Switcher balcony for an inner layer module. The extracted resistance on the supply lines and the expected voltage drop along the balcony is shown in table 7.2.

Net name	Resistance	Voltage drop
VDD	3Ω	$70mV$
VDD_{JTAG}	7Ω	$7mV$
GND	2Ω	$100mV$
per Gate On	0.22Ω	$13mV$
Gate Off	1.3Ω	$80mV$
Clear On	1.3Ω	$80mV$
Clear Off	1.3Ω	$80mV$

Table 7.2: MCM Switcher balcony trace resistances.

7.2.2 End of Stave

The read-out chips DCDB and DHP, the kapton connection and a hole for a screw are located at the end of stave. Many components and traces have to be placed within the constrained space. The signal path has to be routed from the matrix drains through the chips towards the kapton cable. Many power supply lines with high currents, together with the decoupling capacitors have to be arranged. The routing of the Switcher and matrix balcony traces need to be routed on the side of the read-out chips. The four DCDBs occupy already 13.8mm on a silicon width of 15.4mm, leaving $500\mu m$ for routing the matrix bias voltages on the right and 1.1mm on the left for connecting the Switcher supplies to the kapton and the steering signals to the DHP. The DCDBs are placed with a gap of $220\mu m$ between the chips, if the delivered chip size meets the design. But as they are manufactured in a multi-project wafer submission, their size may vary and may increase by up to $65\mu m$ per side. This value has been added as a safety margin and results in a gap of $90\mu m$, if the $65\mu m$ increase is not exceeded. A gap of $90 - 220\mu m$ allows an easy flip-chip placement of the chips.

DCDB

Figure 7.12 display a close-up of the left DCDB, showing the drain fan-out connections on the bottom and the Switcher traces passing by the chip on the left. The DCDB's bump pattern has been optimized for power supply routing on the module. Five bump rows allow the horizontal placement of power buses across all four chips. The drain input bumps are located below these power rails, while the digital I/O and control signals are above. The right sub-figure shows the copper layer with the five rails in the upper half of the DCDB. The routing of the drain lines in the chip's lower half can be seen in the left sub-figure. Blue traces connect the DCDB to the DHP above.

The high power consumption, especially of the DCDs, makes the use of sense lines for the power supplies mandatory. They allow to compensate for the voltage drop on the

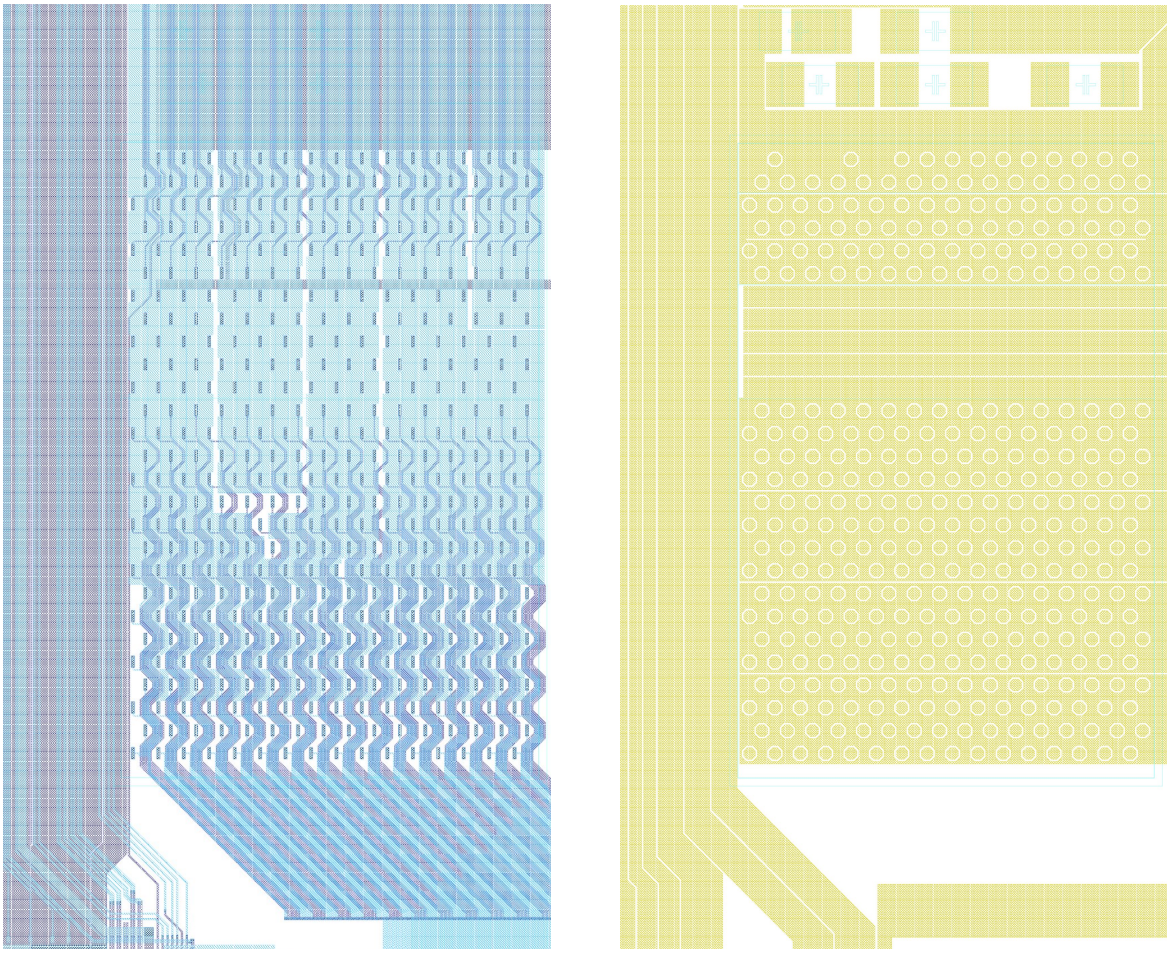

Figure 7.12: Routing of the DCDB and the Switcher balcony for one chip with the first two metal layers in the left and the 3rd copper metal layer on the right picture.

Supply name	**Voltage**	**Current per chip**	**Total current**
AVDD_DCD	1.8V	650mA	2600mA
AGND	0V	500mA	2000mA
DGND	0V	435mA	1740mA
DCD_AmpLow	0.35V	250mA	1000mA
DVDD_DCD	1.8V	250mA	650mA
DVDD_DHPcore	1.2V	145mA	580mA
DCD_RefIn	1.1V	90mA	360mA
DVDD_DHPIO	1.8V	40mA	160mA

Table 7.3: MCM supply currents on the end of stave.

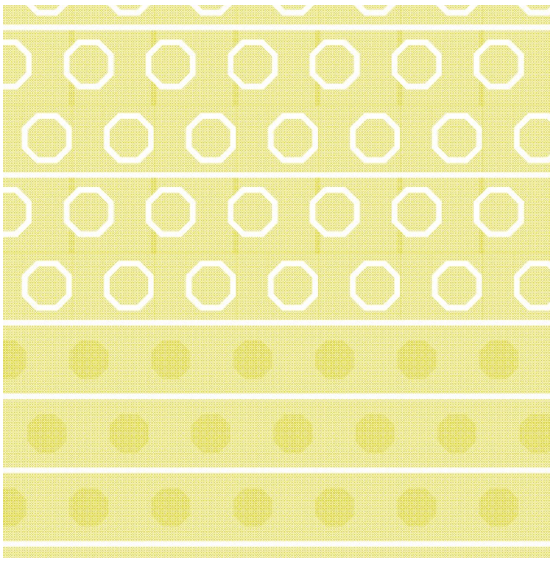

Figure 7.13: Main power buses and additional horizontal metal fill to reduce lateral voltage drop.

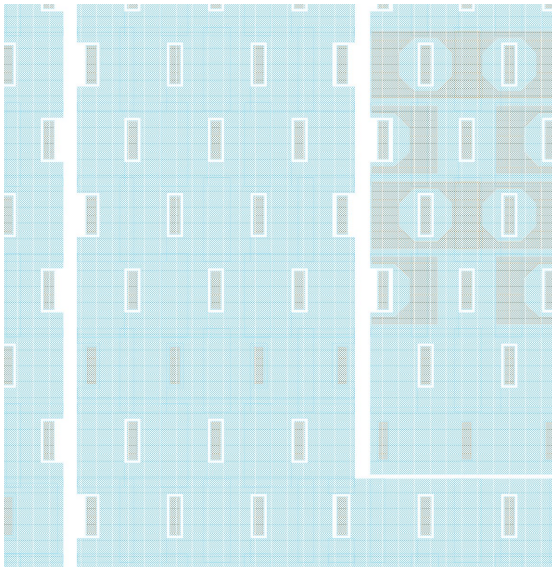

Figure 7.14: Vertical buses on aluminum layer to connect main and additional buses and route the supply nets towards the kapton cable.

cables and on the module routing, by connecting the sense lines as close as possible to the load. The DCDB and DHP supplies are sensed in the middle of the four chips. Additional power buses are placed on the free copper area around the bump pads to reduce the lateral voltage drop across the row of chips (figure 7.13). Vertical aluminum traces connect these additional buses to the main power buses and to the decoupling capacitors placed between DCDB and DHP (figure 7.14). The vertical traces continue below the DHP to route the power towards the kapton. Decoupling capacitors are added for every voltage and are of the same size as used for the Switcher. All voltages are below 4V and allow the use of $220nF$ capacitors, except the decoupling of `AVDD_DCD` to the matrix source voltage.

The width of the via stack connecting the bump pad to the signal traces on the 1^{st} metal layer is horizontally minimized to increase the width of the available aluminum for the vertical supply routing. $480\mu m$ width is achieved for the high current `AVDD_DCD` supply, compared to $270\mu m$ in case of a via matching the bump pad size. The 6-times higher resistivity of the aluminum compared to the copper layer and the electromigration threshold of $2mA/\mu m$ of aluminum, demands for an optimized aluminum power routing.

The resistance from the middle, where the sense lines are connected, to the outermost DCD is $\approx 0.06\Omega$. This reduces the lateral voltage drop across the DCDs.

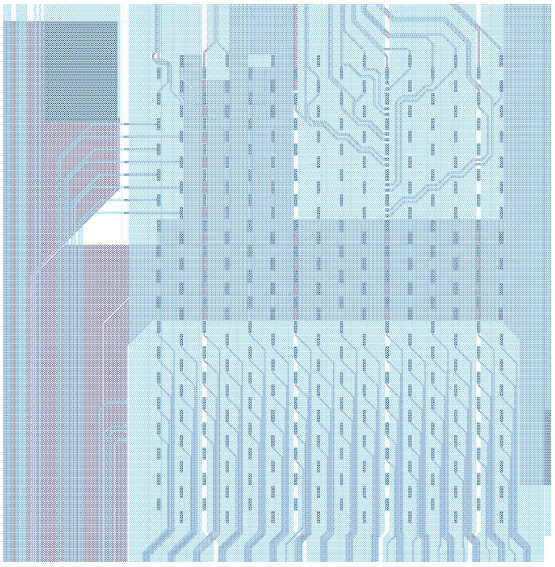

Figure 7.15: Data and control signals and part of the power routed on al1 layer.

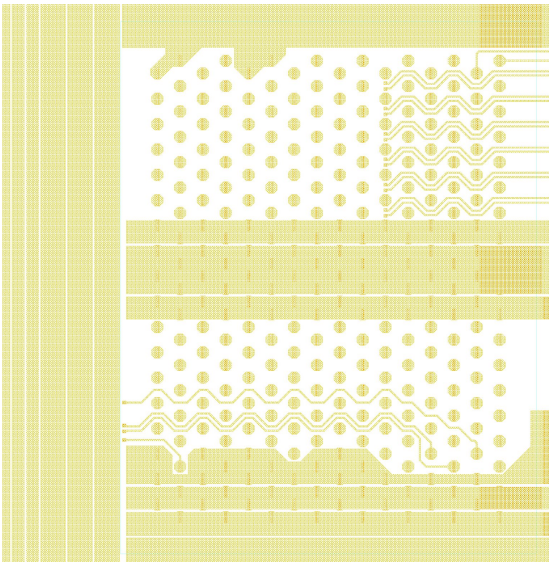

Figure 7.16: Horizontal power distribution on copper layer together with control signals.

DHP

Figure 7.15 shows the first two metal layers. The lower layer is used for connecting the DCDB's signals (lower half of chip) and the DHP control signals (traces entering from top). The Switcher's control and JTAG lines on the left of the chip are connected to appropriate bumps. The JTAG I/O voltage of the Switchers is connected to the DHP's I/O supply to ensure correct voltage levels in the single ended JTAG communication. The second aluminum metal layer is blocked by the DCDB power supply traces. The horizontal DHP power buses shown on the copper layer in figure 7.16 have to be connected by vertical aluminum traces located in the gap between the chips.

Each DHP is equipped with two decoupling capacitors and a termination resistor for the differential chip to chip JTAG interface. The DHP clock and timing signals for frame synchronization and the Belle II detector's trigger signal are also LVDS signals. They are terminated at the right module side. A differential transmission is required, because these signals are also used for off-module communication. They are routed on the copper layer across all chips (figure 7.16 upper half), with termination resistors on the right module side. The copper layer is also used to connect the Switcher JTAG to the DHP.

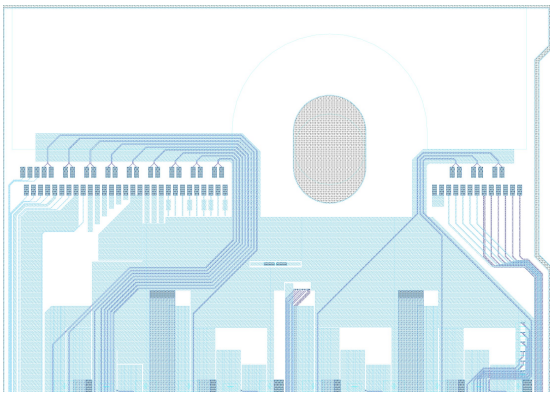

Figure 7.17: Data and control signals on al1 layer. Ends of DCDB power traces and signal shielding on layer al2n.

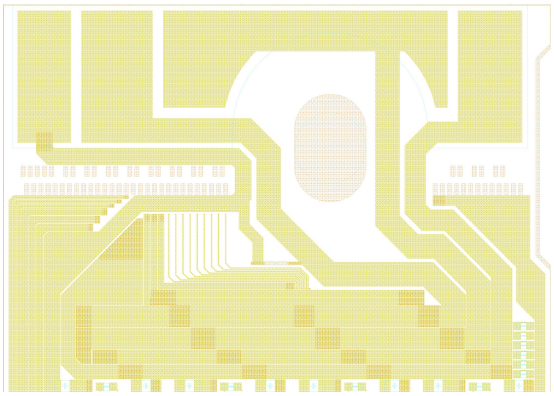

Figure 7.18: Aggregation of DCD and DHP power on copper and routed to the kapton.

Kapton Footprint

A 1.1cm long space is located at the end of the DHPs to place the kapton cable and the wire bond pads required to connect the copper traces on the kapton to the module. A hole or slot in the silicon is used to mechanically mount the silicon module to the support structure. A plastic washer will be used to distribute the screw's forces equally to the silicon and to prevent it from breaking. The kapton's footprint is 14.5mm wide and 4mm long. It has a cut-out to fit around the washer. A three layered kapton will be used. Power traces on the bottom layer carry the high current supplies, the high speed digital traces are in the middle layer and all other signals, voltages and sense lines are on the top layer. The bottom layer will be soldered or glued to the silicon, while the other layers are wire bonded.

The Switcher supply lines can be directly routed to the kapton, while the multiple DCD and DHP supply lines have to be aggregated on the copper layer first. This aggregation blocks a lot of space, but it can't be avoided because the high currents need to routed on the low resistance copper. Four big landing pads are placed below the kapton and connected to the wide aggregation traces using the copper layer only (figure 7.18). Routing on the aluminum layer would require very wide traces to avoid electromigration. The DHP's high speed data outputs and the off-module JTAG connection are routed to the pads bonded to the middle kapton layer. A cover is added above the traces to ensure a more uniform impedance and to shield the lines (figure 7.17).

The wire bond loop height can cause problems with adjacent modules, when the modules are mounted in concentric layers around the beam pipe. The overlapping neighbor module would touch the bond wires. As the layer radius is fixed, the problem can only be resolved by creating a cut-out in the silicon on the right module side.

7.2.3 Active Area Test Structures

The active area is available for test structures, because the MCM is only manufactured with the metal layers. Active devices cannot be implemented due to the missing implantations. Two different designs are manufactured: The first one contains structures for testing the chip's performance in the all-silicon Belle II module. The second design is used for technology yield tests.

The chip test should reveal performance issues that might be caused by the constrained routing space on the module or by the long kapton cable. The flip-chip assembly of the chips onto the thinned silicon and the mounting of the kapton cable can be exercised. Long metal lines are placed in the active area to simulate the capacitive load on the drain, gate and clear signals. A capacitance of $21pF$ is calculated for the 2.7cm long and $8\mu m$ wide drain lines. The DCDB inputs have only been tested with 128 matrix columns with PXD5 or PXD6 matrixes. The crosstalk in between and common mode noise injected to the drain lines can be simulated with the long parallel traces of the MCM. A PXD6 matrix with 128×16 pixels can also be mounted onto the MCM and connected to the drain and steering lines to compare the results of the MCM with the measurements of the hybrid PCBs. $50pF$ is added by the 1.26cm long and $30\mu m$ wide gate and clear lines. Charging this load can simulate the power consumption of a DEPFET matrix, although the additional capacitance of the transistor gates is missing. This can be simulated by load capacitors added to 95 gate and clear lines. Figure 7.19 shows the layout of the active area's lower half with the PXD6 matrix footprint in the lower right. 128 drain lines are connected to the 4 row bond pattern at the top and 16 gate and clear lines are connected to the bond pads at the left of the rectangle. All matrix bias voltages are supplied via the kapton cable. The clear and gate load capacitor footprints are located in the upper left.

The second design contains all metal layers of a Belle II type DEPFET matrix. The anticipated DEPFET cell design is reduced to the metal layers and allows to check the processing yield of the small feature sizes used in the matrix. Much coarser structures have been used for routing on the end of stave and balcony, which relaxes the processing and should result in a higher yield.

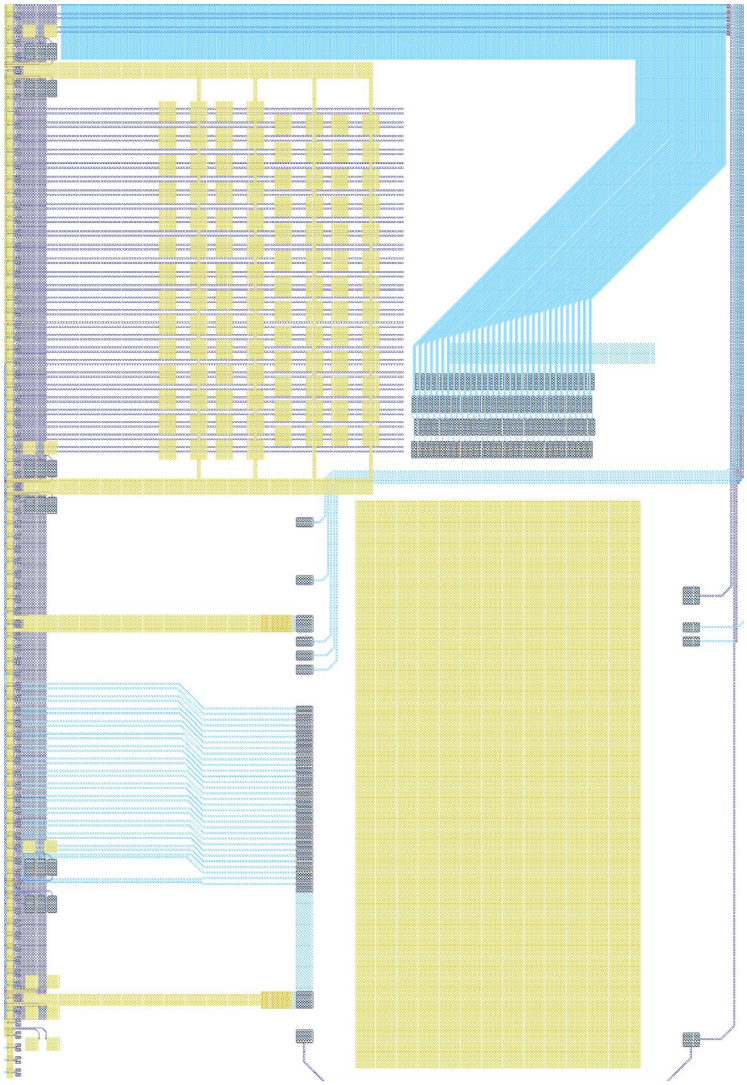

Figure 7.19: Layout in the lower half of the active are test structures with capacitors and PXD6 matrix footprint.

8 Summary and Outlook

The two steering chips Switcher3 and SwitcherB for the ILC and the Belle II experiments have been characterized and irradiated to test their radiation tolerance. Both chips work as anticipated and can be considered radiation hard for the expected dose at the experiments. The flexible sequencer of the Switcher3 can be operated with $150MHz$ and allows the selective region-of-interest read-out of parts of a matrix. The output stage consisting of three stacked 3.3V transistors is capable of providing a 9V swing and can drive the expected matrix load of $22pF$ within $7ns$. An irradiation with an accumulated dose of 10.7Mrad degrades the the operating speed and drive capability as expected. The chip recovers after 40 days of annealing and can be operated with $80MHz$. The expected dose at the ILC detector accumulates to only 200krad within 5 years of operation and thus, the Switcher3 can be considered radiation hard.

The second steering chip designed for the changed requirements of the Belle II detector was characterized and irradiated, too. Threshold voltage shifts of the DEPFET transistor demand extended voltage ranges of the Switcher. The SwitcherB is capable of switching with 50V swing and allows floating supply voltages. A row readout time of $100ns$ can be achieved with the drive capability of $< 10ns$ for the expected matrix load capacitance of $\approx 50pF$. The chip was irradiated up to a dose of 24.5Mrad and is still working with a by $7ns$ slower falling edge. In the Belle II experiment, with a dose rate of 2Mrad/year and 5 years of operation, the chip's falling edge would decrease by $3ns$, whereas the rising edge speeds up by $5ns$. The desired readout speed can still be achieved and the chip can be considered radiation tolerant.

This work contributed also to the read-out chain developments by characterization of the DCD2 read-out chip and development of the DCD-RO converter chip. The new read-out chip family of drain current digitizers (DCD) with a current-only signal path and integrated analog-to-digital conversion has been measured and irradiated. It was shown that the new approach is working with a noise of $\approx 45nA$. The chip was irradiated up to 3.5Mrad. The ADC gain increases slightly and recovers perfectly after 6 days of annealing. The successor of the DCD2 chip requires a signal converter chip to operate for characterization stand-alone. This converter chip was designed during this thesis and is capable of converting single-ended to LVDS signals with up to $400MHz$. It is extensively used in testing of new read-out chip revisions and in the read-out chain of DEPFET matrix test systems.

A flip-chip interconnection technology is mandatory to build a compact all-silicon detector module. Two bumping processes were evaluated and set up in the facilities, which can

accommodate the requirements of the DEPFET module development. The set-up of bumping processes is necessary, because the multi-project chip productions didn't offer commercial bumping. Although it is now possible to order the DCDB with solder bumps, the manual bumping is still necessary for the SwitcherB chips. It is also required for test chips with improved DCDB circuits to reduce the manufacturing costs for these submissions. The chosen bumping processes are flexible and can be easily adopted to new layouts. They allow the processing of chips with a standard aluminum pad finishing and eliminate special pre-treatments. The gained bumping knowledge is transferred to other projects too, which develop novel hybrid detector assemblies or flip-chip connect read-out chips and detectors to interposers, as presented in chapter 6.7.

Another vital step in the construction of an all-silicon detector module is the demonstration of the feasibility to interconnect all module components. The read-out and steering chips have to be connected to the DEPFET pixel matrix and the power and data signals have to be connected off-module. The first all-silicon layouts have been designed and were manufactured with the PXD6 DEPFET test production. The module sizes and technological options differ from the final properties for the Belle II detectors, but the modules might reveal problems which can be addressed in the upcoming chip and detector developments.

The development of the Multi Chip Module is the first design combining all components of the Belle II detector module. The silicon dimensions, DEPFET matrix size, chip locations and kapton size are representing the final geometry. Only the active area has to be filled with active DEPFET devices in the upcoming development run. Many more chips and traces are required on a smaller silicon area, in comparison to the PXD6 production, to build these modules. A layout was successfully designed which incorporates all necessary traces into the confined area. Active DEPFET devices are omitted to reduce the production time. All chips will be flip-chip soldered on the Multi-Chip Module, the kapton cable will be attached and two thinned modules will be glued together to present the first electrically active DEPFET ladder for the Belle II pixel vertex detector.

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