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Results of On-Line Tests of the ENABLE Prototype, a 2nd Level Trigger Processor for the TRD of ATLAS/LHC

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Abstract

The Enable Machine is a systolic 2nd level trigger processor for the transition radiation detector (TRD) of ATLAS/LHC. The task of the processor is to find the best candidate for a lepton track in a high background of pions according to the EAST benchmark [2] in less than 10 μs. As described earlier [1, 2] the Enable Machine finds all reasonable tracks by histogramming the coincidence of the mask templates and the RoI for each track.

A prototype has been developed and tested within the EAST/RD-11 collaboration at CERN. It operates at 50 MHz and finds up to 400 arbitrary tracks in less than 10 μs. It is assembled of an interface board and one or more histogrammer boards which makes the Enable Machine easily scalable. The histogrammer units are systolic arrays consisting of a matrix of 36 field-programmable gate arrays (Xilinx XC3190). Through this it is possible to optimize the trigger algorithm, to adapt it to a changed detector setup, and it allows even the implementation of completly new algorithms.

For the beam tests in autumn 1993 at CERN the overall functionality within the detector environment could be shown. We were able to link successfully the Enable prototype to the detector raw data stream as well as to the data acquisition system. For the next beam period in 1994 we will focus on efficiency measurements and tests with maximal detector data rate.

1. Introduction

Second level trigger algorithms often are quite similar. Normally they require moderately complex pattern recognition combined with a very high data rate while they show up a high degree of parallelism.

Systolic arrays consisting of a matrix of field-programmable gate arrays are well suited to such problems. With their internal structure of up to 1000 processor elements (PE's) and flip-flop toggle rates of 100 MHz, the use of reprogrammable logic provides great flexibility and high speed.

In this paper we want to present a prototyp Enable Machine, a high speed pattern recognition processor using the advantages of building processors with matrices of FPGAs. We want to describe the architecture and the implementation of the prototyp and present first results from data taken during the beam period in autumn 1993.

2. Algorithm

As described somewhere else [3] every 10 μs a subset of the whole detector image, called Region of Interest (RoI) is selected by the 1st level trigger (calorimeter) and analysed by the 2nd. In this subset particle tracks appear as straight lines of different slope due to their transversal momentum.

The trigger task is to find the most reasonable lepton track and to evaluate its transversal momentum.

The Enable Machine finds tracks by histogramming the coincidence of image data and predefined search roads. The maximal slope of search roads defines the p_t cut. According to low and high threshold hits for every search road, two separate histograms are computed. The particles are separated by the ratio of these two corresponding histogram channel contents.

The Maximum of a weighting function of all contents is evaluated to determine the strongest lepton track.

3. Implementation

The main processing unit of the Enable machine consists in a matrix of 36 Field Programmable Gate Arrays (FPGAs) of type Xilinx XC3190. The use of FPGAs has two impotant advantages: It increases speed by executing the algorithm in hardware and provides flexibility by reconfiguration of the FPGAs. For additional flexibility search roads are controlled by activation RAM and the weighting function is implemented in lookup tables.

Due to the inherent parallelism of the TRD algorithm the Enable machine's architecture is massively parallel and pipelined. Image column are

handled in parallel, different slopes in a pipeline (fig.1).

The Enable machine runs with a clock frequency of 50MHz that allows a maximal data throughput of 400 MByte/s. Depending on the image dimensions the processing time is between 1µs and 6µs (z=1 .. 256). One FPGA-matrix allows the parallel search for 400 pattern.

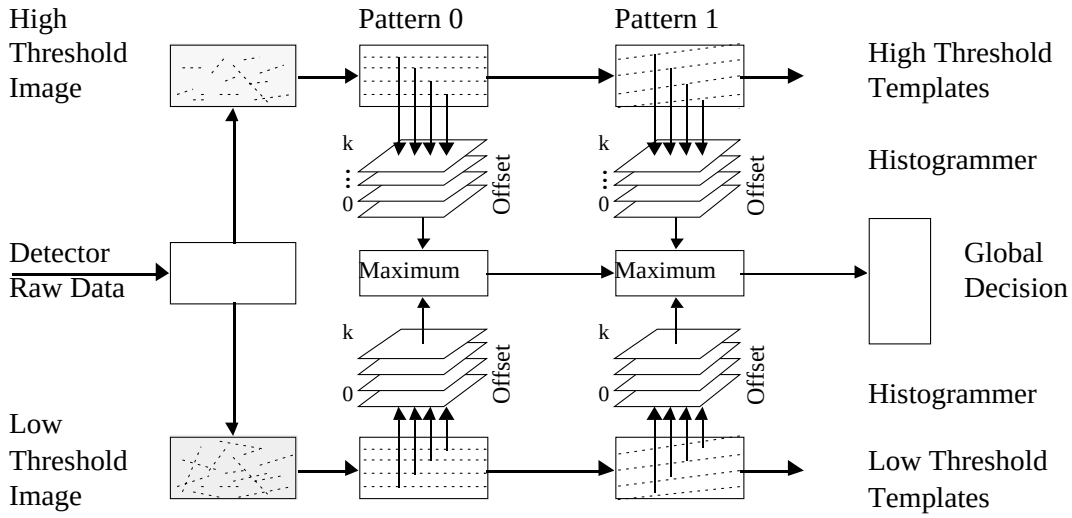

Figure 1

4. Hardware Setup

The prototype Enable Machine is assembled of an interface board and one or more histogrammer boards (one for the test setup).

Event data are received by two HIPPI channels on the interface board and broadcasted to the histogrammer units. In the histogrammer units the event is processed and transmitted back to the interface board. Here the results from each histogrammer board are combined to the global trigger decision of the Enable Machine. This modular concept makes the Enable Machine easily scalable from 400 to 8000 patterns where each pattern corresponds to one possible electron track.

Event data, i.e., region-of-interest (RoI) images of size 256*32*2 bit, are received by the Enable Machine's interface board via two HIPPI lines that provide a maximal input data rate of 200 MB/s. The HIPPI destination interface assembled on the interface board has been developed with Dubna/Russia in a joint project.

A histogrammer unit of the Enable Machine mainly consists of a matrix of 36 gate array devices of type Xilinx XC3190 and over 4 MBytes of synchronous SRAM for pattern definition and lookup tables. For debugging and monitoring purposes the full histogram content can be read out from the histogrammer board via VME. Like for the interface board it is also possible to download events from the VME host and to process them.

The whole system houses in a VME crate. The board size is 40*38 cm2 (6 height units). The Enable Machine is controlled and programmed by a commercial VME module containing a µSPARC processor. It is used as the bus master whereas the Enable boards are only VME slaves (fig. 2). This is sufficient for trigger purposes.

5 System Embedding

For the beam tests in autumn 1993 at CERN the Enable Machine was embedded in a special test environment of the TRD. The Enable machine was not directly coupled to the detector data but to the TRD router, a special system that copied RoI windows out of the detector data stream and send it to the Enable machine via 2 HIPPI links.

The Enable VME crate was coupled to the data aquisition crate via a VIC bus module containing 4MB of memory. During bursts the memory was filled by Enable. In the time gap between bursts the data aquisition system read this buffer.

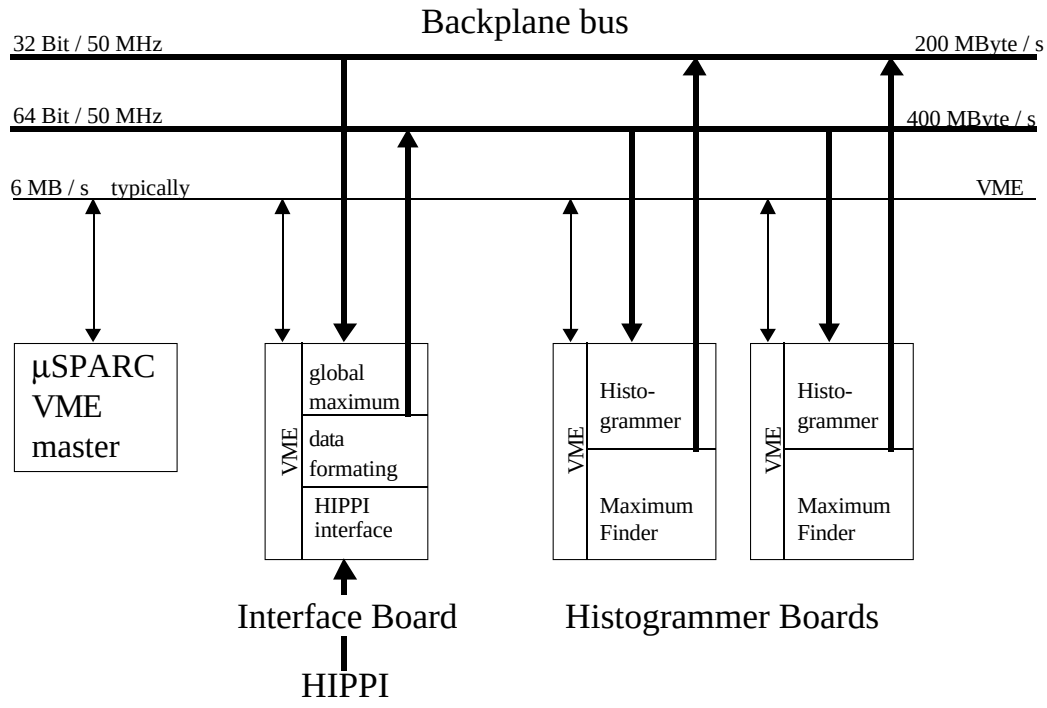

Figure 2

6 Results from the beam period 1993

For the beam tests in autumn 1993 at CERN it was intended to show the overall functionality within the detector environment. This comprised data input handling, correct histogramming of events and connection to the data acquisition system.

The Enable Machine is the first 2nd level trigger processor developed for ATLAS which was tested under beam conditions. During the run the Enable Machine could be successfully integrated in the test detector data acquisition system and 10^5 events could be recorded on tape.

It was possible to forward a continous event data stream from the detector through the router to the Enable Machine, although several problems were encountered. The main problems arose because error handling between the units was poorly defined and due to synchronization faults of the two HIPPI lines.

Offline analysis verified that apart from some minor bugs both the z-f corner turning as well as the histogrammer produced correct results.

Nevertheless it was possible to identify events with the corresponding raw event data which proved that the transfer from the detector through the router to the Enable Machine worked correctly.

So the principle functionality of the Enable Machine could be shown.

7 Outlook

The pattern recognition task for most 2nd level trigger problems are of moderate complexity, offer a high degree of parallelism, and have to deal with very high data rates. For these kinds of requirements a FPGA-processor like the Enable machine with its massively parallel architecture is very well adapted. The execution in hardware provides additional speed.

But apart from traditional hardware solutions that were fixed to one certain problem reconfigurable FPGAs offer a new quality. The massive use in form of a FPGA-matrix allows the reconfiguration of the whole processor. Reconfiguration can be used to implement different trigger algorithms onto a single machine. We have started to investigate in the implementation of several LHC 2nd level trigger algorithms on Enable in order to extract an optimal architecture for a general purpose FPGA-matrix.

It is intended to build up such a processor with a more generalized architecture. That general

purpose machine will be available end of 1995 and will be able to solve most LHC 2nd trigger problems.

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[2] Badier J., Bock R.K., Busson Ph., Centro S., Charlot C., Davis E.W., Denes E., Gheorghe A., Klefenz F., Krischer W., Legrand I., Lourens W., Malecki P., Männer R., Natkaniec Z., Ni P., Noffz K.-H., Odor G., Pascoli D., Zoz R., Sobala A., Taal A., Tchamov N., Thielmann A., Vermeulen J., Vesztergombi G.: Evaluating Parallel Architectures for two Real-Time Applications with 100KHz Repetition Rate; IEEE Tr. Nucl. Sci., Vol. 40, No. 1 (1993) 45-55

[3] Klefenz F., Männer R., Noffz K.-H., Zoz R.: EAST note 92-01